

Board Level Reliability of Lead-Free Solder Interconnections with Solder Doping Under Harsh Environment

by

Cong Zhao

A dissertation submitted to the Graduate Faculty of
Auburn University
in partial fulfillment of the
requirements for the Degree of
Doctor of Philosophy

Auburn, Alabama
August 5, 2017

Keywords: Reliability, Lead-Free Solder, Solder Doping, Isothermal Aging,
Electronics Packaging, Failure Analysis

Copyright 2017 by Cong Zhao

Approved by

John L. Evans, Chair, Charles D. Miller Endowed Chair of Industrial and Systems Engineering
Michael Bozack, Professor, Physics
Gregory Harris, Associate Professor, Industrial and Systems Engineering
Sa'd Hamasha, Assistant Professor, Industrial and Systems Engineering

Abstract

The electronics packaging industry has moved from eutectic Sn-Pb solder to the lead-free near-eutectic Sn-Ag-Cu (SAC) solder system in the past few years. Reliability performance for Lead-Free solder joint under “extreme” or “harsh” environments, for example exposition to long-term isothermal aging in elevated temperature and thermal cycling, has been studied and examined. Previous studies show reliability of Ball Grid Array (BGA) packages with SAC105 and SAC305 solder joints can degrade up to 70% after aging at 125°C for 24 months. People in industry have begun to consider the effect of long-term isothermal aging on the reliability of Lead-Free solder joint. Many solutions targeting applications in harsh environments requiring resistance to both thermo-mechanical (accelerated thermal cycling) and mechanical (vibration, bending, and shock) loading have been proposed. One possible solution is to develop a “next generation” solder alloy with additional elemental dopants metal mixed with SAC lead-free solder family, such as antimony (Sb), magnesium (Mg), nickel (Ni), cobalt (Co), or indium (In). These additives create finer grain boundaries and reduce the intermetallic formations of the tin with silver or copper, resulting in a more reproducible grain as well as a more uniform grain formation in the lead-free alloy. This process is called solder doping. So the purpose for this project is to firstly find a manufactureable solder paste with dopants that can mitigate the effects of aging. A secondary goal is to find a solder material for solder-sphere replacement to enhance individual package reliability.

This dissertation presents harsh environment reliability test results for lead-free, principally Tin-Silver-Copper (SAC) based solder pastes with and without the presence of a variety of dopant elements (Bi, Sb, Ni, Mn, Nd, and In). SAC105 and SAC305 solder alloy spheres are mixed with 14 different doped solder pastes and subsequently tested under long-term isothermal aging and thermal cycling condition in order to evaluate the ability of solder doping to mitigate the effect of aging and to enhance the solder joint reliability. In addition to BGAs with package size ranging from 15mm (0.8mm pitch) to 6mm (0.8mm pitch), the test vehicle also incorporates no-lead packages such as Quad Flat No-leads (QFNs) and 2512 Surface Mount Resistors (SMRs). Three surface platings are tested: Organic Solderability Preservative (OSP), Immersion Silver (ImAg), and Electroless Nickel Immersion Gold (ENIG). All test vehicles were subjected to isothermal aging at temperatures of 125°C with aging time of either 0 or 12 months, followed by accelerated thermal cycle (ATC) testing from -40°C to 125°C. This dissertation presents results for the first 2700 thermal cycles. Current reliability data indicates that 8 doped solder pastes demonstrate superior reliability, which can help improving the reliability of lead-free solder under aging, while 4 pastes have somewhat lower performance. Solder pastes with good performance tend to have high Ag content (>3.0%), Bi content (>3.0%), and Sb content (>1.5%). Failure analysis shows continuous growth of Intermetallic Compounds (IMC) at solder joint-pad interface and within the solder bulk. For solder pastes that contain high Silver content, large plate-like Ag_3Sn bulk IMC can usually be noticed, together with particle-like Cu_6Sn_5 bulk IMC, which can sometimes block the propagation of cracks through solder bumps, thus pastes with high silver content tends to have higher reliability. IMC thickness analysis shows that during thermal aging and cycling, the IMC layer in both the component- and board-side interfaces thicken continuously, consuming material from the copper pads and solder joint. ENIG finish can limit

the IMC layer thickness, because it has an additional nickel layer between solder joint and Printed Circuit Board (PCB) copper pad, which acts as a diffusion barrier preventing copper dissolution into the solder. Solder pastes with high bismuth ($>3\%$) and silver ($>3\%$), can help limit the growth of the IMC layer thickness, as well as prevent copper diffusion from the PCB copper pad into solder joint, hence help stabilize and strengthen the interfacial IMC layer and improve reliability performance. Crack propagation is observed in the component-side, near interfacial regions in some materials and through the bulk solder in other materials. 2512 Surface Mount Resistors sampled thus far demonstrate typical fatigue crack propagation mechanics from the inside out through the main fillet. Polarized Light Microscope (PLM) images show recrystallization phenomenon in the solder bulk.

Acknowledgments

The author would like to acknowledge his advisor Dr. John L. Evans for his support, guidance, and mentorship throughout this research. Sincere gratitude and appreciation are also extended to my committee members, Dr. Mark L. Adams, Dr. M. J. Bozack, Dr. Gregory Harris, and Dr. Sa'd Hamasha for their valuable insights and precious time in the course of this research. The author particularly thanks Dr. Michael Bozack for his editorial guidance during the publication of several journal papers and this thesis, with many useful discussions during the lead-free soldering project. Thanks are also extended to all my lab-mates, coworkers, and friends: Dr. Thomas Sanders, Dr. Zhou Hai, Dr. Chaobo Shen, Francy John Akkara, Anto Raj, Sharath Sridhar, Seth Gordon, Sinan Su, and thank you Dr. Michael Miller and Mr. John Marcell for your encouragement and friendship. Finally, the author is in debt to his parents who have supported him endlessly although they are so far away.

Table of Contents

Abstract	ii
Acknowledgments	v
Table of Contents	vi
List of Tables	ix
List of Figures	x
List of Abbreviations	xv
Chapter 1	- 1 -
General Introduction to Electronic Packaging	- 1 -
1.1 Electronic Packaging	- 1 -
1.2 Electronic Components	- 3 -
1.2.1 THMT Components	- 3 -
1.2.2 SMT Components	- 4 -
1.2.3 Leaded Components	- 4 -
1.2.4 No-Leads Components	- 6 -
1.2.5 BGA (Ball Grid Array)	- 7 -
1.2.5 PGA (Pin Grid Array)	- 11 -
1.2.5 LGA (Land Grid Array)	- 12 -
1.3 Substrate for Electronic Packaging	- 12 -
1.3.1 Substrate Material	- 13 -
1.3.2 Solder Mask	- 15 -
1.3.3 Surface Finish	- 16 -
1.4 Solder Alloy	- 19 -
1.4.1 Tin-Lead Solder	- 20 -
1.4.2 Lead-Free Solder	- 22 -

1.4.3 New Solder Alloy and Solder Doping.....	- 24 -
1.5 SMT Assembly Process	- 26 -
1.6 Outline of the Proposal Dissertation	- 33 -
Chapter 2	- 34 -
Literature Review.....	- 34 -
2.1 Introduction	- 34 -
2.2 Effect of IMC on the Reliability	- 36 -
2.2.1 Ag ₃ Sn IMC	- 37 -
2.2.2 Cu-Sn IMC	- 39 -
2.2.3 Ni-Sn IMC	- 42 -
2.3 Effect of CTE	- 43 -
2.4 Grain Recrystallization.....	- 45 -
2.5 Statistical Weibull Analysis Of Reliability.....	- 48 -
2.6 Failure Modes	- 50 -
2.7 Accelerated Life Testing.....	- 52 -
2.8 Solder Doping.....	- 56 -
Chapter 3	- 57 -
Experimental Setup.....	- 57 -
3.1 Introduction	- 57 -
3.2 Test Vehicle (TV) Design and Assembly	- 58 -
3.2.1 Test Board Design (TV9)	- 58 -
3.2.2 Test Components	- 61 -
3.2.3 Solder Pastes.....	- 62 -
3.2.4 TV SMT Assembly.....	- 64 -
3.3 Thermal Test	- 66 -
3.3.1 Isothermal Aging and Thermal Cycling Test Matrix	- 66 -
3.3.2 Data Acquisition System	- 68 -
3.3.3 Failure Analysis.....	- 70 -
Chapter 4.....	- 71 -
Reliability Data Analysis	- 71 -
4.1 Introduction	- 71 -

4.2 Data Analysis	- 71 -
4.2.1 Failure Percentage	- 71 -
4.2.2 Weibull Plots and Degradation Charts	- 73 -
4.2.2.1 Reliability Performance of All Solder Pastes	- 73 -
4.2.2.2 Reliability for BGA Package with Different Solder Spheres	- 80 -
4.2.2.3 Reliability for BGA Package with Different Surface Finishes.....	- 88 -
4.2.2.3 Reliability for BGA Package with Aging Effect.....	- 95 -
4.2.2.4 Reliability for 2512 SMR Package.....	- 99 -
Chapter 5	- 103 -
Failure Analysis	- 103 -
5.1 Introduction	- 103 -
5.2 Typical Microstructure of SAC BGA Solder Joint	- 103 -
5.3 Microstructure of 15mm BGA Solder Joint with Paste B.....	- 105 -
5.4 Microstructure of 15mm BGA Solder Joint with Paste F	- 109 -
5.5 Microstructure of 15mm BGA Solder Joint with Paste A	- 112 -
5.6 Crack Propagation and Failure Modes	- 117 -
5.7 IMC Growth and Thickness Analysis	- 124 -
Chapter 6.....	- 130 -
Results and Conclusions	- 130 -
6.1 Results and Conclusions	- 130 -
6.2 Future Work	- 133 -
References.....	- 135 -

List of Tables

Table 1.1 Main Types of Gull Wing and J-Lead Packages [3].....	5
Table 1.2 Engineering properties of FR-4	14
Table 1.3 Summary of properties of surface finishes	18
Table 1.4 Summary of properties to be considered for solder alloy selection [25]	20
Table 2.1 Cost of failure for different types of business [49]	34
Table 2.2 Factors that affect BGA solder joint reliability	36
Table 2.3 Typical CTE.....	45
Table 2.4 Dwell temperatures for TC testing by application [83]	54
Table 3.1 Test component matrix	62
Table 3.2 Solder paste information	63
Table 3.3 Isothermal aging test matrix (tabular number stands for number of test vehicles).....	67
Table 4.1 Package failure percentages with aging (2700 thermal cycles)	72
Table 4.2 Package failure percentages without aging (2700 thermal cycles)	72
Table 5.1 IMC layer thickness growth for a 19mm BGA package with Paste I and OSP finishes	124

List of Figures

Figure 1.1 Hierarchy of interconnection levels.....	1
Figure 1.2 A DIP and its side view	3
Figure 1.3 Gull Wing component (a) and J-Lead component (b).....	5
Figure 1.4 SMR component (a) and QFN component (b)	6
Figure 1.5 Side view of QFN component	7
Figure 1.6 Top and bottom side of a BGA component.....	8
Figure 1.7 Cross-Section view for a PBGA component.....	9
Figure 1.8 Cross-Section view for a CBGA component.....	9
Figure 1.9 Cross-section view for a TBGA component	10
Figure 1.10 Cross-section view for a standard BGA (left) and cavity down BGA (right)	10
Figure 1.11 Comparison of a standard BGA (top) and a CSP (bottom)	11
Figure 1.12 A PGA component used in Motorola 68020 microprocessor	11
Figure 1.13 Schematic comparison of PGA (top), LGA (middle), and BGA (bottom)	12
Figure 1.14 Cross-section view of a PCB with different types of vias: (1) through hole; (2) blind via; (3) buried via. The green and gray layers are non-conducting, while the thin orange layers and vias are conductive.....	13
Figure 1.15 Top view (Left) and cross-section view (right) of NSMD versus SMD PCB.....	15
Figure 1.16 Cross-section view of a PCB with surface finish applied on copper pad.....	16
Figure 1.17 Phase diagram for tin-lead solder alloy	21
Figure 1.18 Market share of lead-free alloys (a) and SAC alloys (b).....	26
Figure 1.19 Typical SMT assembly process flow	27
Figure 1.20 A picture of solder paste.....	27
Figure 1.21 A picture of stencil printer (a) and cross-section view of a squeegee printing solder paste on stencil.....	28
Figure 1.22 Example of fault found by 2D inspection.....	29

Figure 1.23 Different types of unsatisfied printing result.....	29
Figure 1.24 (a) Example of a reflow oven (b) with its cross-section view of structure.....	30
Figure 1.25 A typical reflow thermal profile	31
Figure 1.26 A typical SMT assembly production line	32
Figure 2.1 Binary phase diagram for Sn-Ag [59]	37
Figure 2.2 Ag ₃ Sn Morphology: particle-like (a), needle-like (b), and plate-like (c) [60]	38
Figure 2.3 The initial microstructure of Sn-xAg-Cu bulk solders [61]	38
Figure 2.4 Initial morphology of the η -phase Cu ₆ Sn ₅ upon cooling: (a) water quenching, (b) air cooling, and (c) furnace cooling [66].....	40
Figure 2.5 Intermetallic morphology development during aging at 140°C [66]	40
Figure 2.6 IMC at the interface of copper pad and SAC405 after 32 days of aging at 150°C [68] 7	
Figure 2.7 Microstructure change of the IMC layer at solder/Ni interface under different aging times, (a) 0 h, (b) 120 h, (c) 260 h and (d) 500 h [70]	42
Figure 2.8 Interface of solder-HASL pad interface (a) and solder-ENIG interface (b) after 1000 hours of aging [71].....	43
Figure 2.9 DNP model [3]	44
Figure 2.10 Dynamic recrystallization of Sn-rich during thermal cycling (a) as reflowed, (b) 500 thermal cycles, (c) 1500 thermal cycles [71]	46
Figure 2.11 Sn Grain Boundaries Under Cross Polarized Light [72]	47
Figure 2.12 Recrystallization phenomenon [72].....	48
Figure 2.13 Weibull plot for 19mm BGA SAC305 on ImAg aging at 125°C up to 24 months [74]	49
Figure 2.14 Common BGA solder joint failure modes: crack propagates along near-interfacial IMC layer (a), and crack propagates through bulk solder [75].....	51
Figure 2.15 Typical failure mode for surface mount resistor [76].....	51
Figure 2.16 Temperature profile for thermal cycle test conditions [78].....	52
Figure 2.17 Characteristic life degradation chart for BGA SAC solder joints with various aging times (a) and temperatures (b)	55
Figure 3.1 Test board design of frontside (a) and backside (b)	59
Figure 3.2 RBS for surface finishes: (a) ENIG, (b) ImAg, (c) OSP	60
Figure 3.3 Bottom view of BGA package: (a) full array 6mm BGA, (b) perimeter 15mm BGA	62
Figure 3.4 SMT assembly line at UAH	64

Figure 3.5 Reflow oven.....	65
Figure 3.6 Reflow profile.....	66
Figure 3.7 Thermal cycling test profile.....	68
Figure 3.8 (a) Thermal cycling chamber with test vehicles inside and (b) connected data acquisition system.....	69
Figure 3.9 Schematic design of the monitoring system.....	69
Figure 4.1 Weibull plot for 15mm BGA package with SAC105 solder sphere and OSP surface finish on all solder pastes.....	74
Figure 4.2 Degradation chart for 15mm BGA package with SAC105 solder sphere and OSP surface finish on all solder pastes.	75
Figure 4.3 B10 life degradation chart for 15mm BGA package with SAC105 solder sphere and OSP surface finish on all solder pastes.	76
Figure 4.4 Weibull plot for 15mm BGA package with SAC105 solder sphere and ImAg surface finish on all solder pastes.....	77
Figure 4.5 Degradation chart for 15mm BGA package with SAC105 solder sphere and ImAg surface finish on all solder pastes.	78
Figure 4.6 B10 life degradation chart for 15mm BGA package with SAC105 solder sphere and ImAg surface finish on all solder pastes.	79
Figure 4.7 Weibull Plots for the 15mm BGA with paste A after aging on each surface finish: (a) ImAg surface finish, (b) OSP surface finish, (c) EING surface finish	82
Figure 4.8 Characteristic life values for 15mm BGA with paste A.....	83
Figure 4.9 Weibull plots for the 15mm BGA with paste I after aging on each surface finish: (a) ImAg surface finish, (b) OSP surface finish, (c) EING surface finish	85
Figure 4.10 Characteristic life values for the 15mm BGA with Paste I	85
Figure 4.11 Weibull plots for the 15mm BGA with (a) Paste B & OSP finish, (b) Paste G & OSP finish, (c) Paste G & ImAg finish	87
Figure 4.12 Characteristic life values for the 15mm BGA with Paste B & OSP finish, Paste G & OSP finish, and Paste G & ImAg finish	88
Figure 4.13 Weibull plots for 15mm BGA with Paste A on each surface finish for (a) matched paste and spheres, (b) Paste A with SAC105 spheres, (c) Paste A with SAC305 spheres	90
Figure 4.14 Characteristic life values For 15mm BGA with Paste A on each surface finish.....	90
Figure 4.15 Weibull plots For 15mm BGA with SAC105 sphere on each surface finish for (a) Paste H, (b) Paste F, (c) Paste G	92

Figure 4.16 Characteristic life values for 15mm BGA SAC105 sphere with Paste F, Paste G and Paste H	93
Figure 4.17 Weibull plots for 15mm BGA with Paste A on each surface finish for (a) Paste I with SAC105 spheres, (b) matched paste and spheres,.....	94
Figure 4.18 Characteristic life values for 15mm BGA with Paste I on each surface finish	95
Figure 4.19 Weibull plots for 15mm BGA with different surface finishes considering aging effect (a) Paste B with SAC105 spheres, (b) Paste B with SAC105 spheres, (c) Paste C with SAC105 spheres.....	97
Figure 4.20 Characteristic life values for 15mm BGA considering aging effect	97
Figure 4.21 Weibull plots for 2512 SMR with Paste F, G, L, and A on each surface finish: (a) ENIG, (b) ImAg, (c) OSP.	100
Figure 4.22 Characteristic life values for 2512 SMR with Paste A, F, G, and I: (a) paste comparison, (b) surface finish comparison.....	101
Figure 5.1 Typical microstructure of SAC solder joint with ImAg or OSP finish	104
Figure 5.2 Typical microstructure of SAC solder joint with ImAg or OSP finish	105
Figure 5.3 illustrates the plate-like Ag ₃ Sn IMC and particle-like Cu ₆ Sn ₅ IMC inside the solder bulk, together with Cu ₆ Sn ₅ IMC layer in the package side. Figure 5.4 shows a magnified image of the microstructure of a 15mm BGA Package with Paste B and OSP surface finish.....	106
Figure 5.4 Higher magnification SEM and EDX of microstructure for 15mm BGA package with Paste B: (a) IMC layer, (b) plate-like and particle-like Ag ₃ Sn bulk IMC, (c) particle-like Cu ₆ Sn ₅ bulk IMC	107
Figure 5.5 Microstructure for 15mm BGA package solder joint with Paste B: (a) polarized light microscope image, (b) SEM image.....	109
Figure 5.6 SEM and EDX of microstructure for a 15mm BGA package with Paste F and ImAg finish: (a) plate-like and particle-like Ag ₃ Sn bulk IMC, (b) Cu ₆ Sn ₅ bulk IMC and IMC layer	110
Figure 5.7 Polarized light microscope image of microstructure for a 15mm BGA package solder joint with Paste F including “Beach Ball” structure	111
Figure 5.8 SEM and EDX of microstructure for 15mm BGA package with Paste A and OSP finish: (a) matched sphere with plate-like Cu ₆ Sn ₅ bulk IMC, (b) SAC305 sphere with particle-like Ag ₃ Sn and Cu ₆ Sn ₅ bulk IMC, (c) SAC105 with particle-like Cu ₆ Sn ₅ bulk IMC.....	114
Figure 5.9 SEM and EDX of microstructure for 15mm BGA package with Paste A and ENIG finish: (a) particle-like (Cu, Ni) ₆ Sn ₅ bulk IMC and IMC layer, (b) nickel layer for ENIG finish	117
Figure 5.10 Typical failure modes for BGA package. Crack propagation close to the (a)(b) board-side and package-side IMC layer. (c)(d) Crack propagation through the solder bulk.	120

Figure 5.11 shows clearly how main the crack and sub-cracks propagate along recrystallized grain boundaries.....	122
Figure 5.12 Failure mode for 2512 surface mount resistor.....	123
Figure 5.13 IMC layer thickness growth for 19mm BGA package with Paste I and OSP finishes with the increase of thermal cycles.....	125
Figure 5.14 Comparison of board side IMC layer thickness at 2600 thermal cycles for Paste A with: (a) ImAg finish, (b) OSP finish, (c) ENIG finish	126
Figure 5.15 Comparison of board side IMC layer thickness for Paste C with: (a) no aging, (b) 12 month aging at 125°C (measured at 2600 Thermal Cycles).....	127
Figure 5.16 Comparison of board side IMC layer thickness for (a) Paste B OSP finish match sphere: (a) Paste F ImAg finish match sphere, (c) Paste I OSP finish match sphere	128

List of Abbreviations

BGA	Ball Grid Array
QFN	Quad Flat No-lead
IMC	Intermetallic Compounds
OSP	Organic Solderability Preservative
ENIG	Electroless Nickel Immersion Gold
ImAg	Immersion Silver
SAC	Tin-Silver-Copper
PCB	Printed Circuit Board
PLM	Polarized Light Microscope
SMR	Surface Mount Resistor
THMT	Through-Hole Mount Technology
SMT	Surface Mount Technology
SEM	Scanning Electron Microscope
CTE	Coefficient of Thermal Expansion
EDX	Energy-Dispersive X-Ray Spectroscopy
FEA	Finite Element Analysis

Chapter 1

General Introduction to Electronic Packaging

1.1 Electronic Packaging

The electronic packaging industry is the largest industry in the world [1]. Over the past few years, consumer electronics such as smartphones and wearables, have totally changed the way people interact with each other. Those electronics also bring significant challenges to the electronic packaging world, by reduced product size and increased design complexity [2]. Basically, electronic packaging provides housing and interconnection of integrated circuits to form electronic systems. Electronic packaging is a multi-disciplinary subject, and includes a wide variety of technologies from mechanical, electrical and industrial engineering, chemistry, physics and even marketing [3]. There are several functions of electronic packaging [4]:

1. Circuit support and protection
2. Heat dissipation
3. Signal distribution
4. Power distribution

Electronic packaging includes different hierarchy of interconnection levels, which is shown in Figure 1.1.

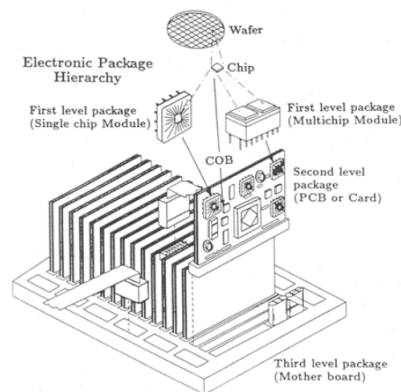


Figure 1.1 Hierarchy of interconnection levels

Level 0 is the gate-to-gate interconnections on the silicon die, or chip. A silicon die is diced from a single-crystal silicon wafer, which contains millions of solid-state semiconductor devices (transistors, capacitors, inductors, and resistors) that have been connected to form functional electrical circuitry [5]. Level 1 is the comprised of connections from the die to its package, or chip carrier. Typically, the silicon die is mechanically attached to a lead-frame or interposer layer, and electrically connected to its carrier by wire bonding or flip-chip BGA. Level 2 is connections from component to component, or to an external connector, which is called as printed circuit assembly (PCA). Printed circuit assembly is based on a substrate, usually called a printed circuit board, or PCB. The PCB provides mechanical support, thermal dissipation, as well as electrical connections to components [6]. The components are attached to the substrate using solder joints, which are metal alloys providing metallurgical bond between components and the PCB to form electrical, mechanical, and thermal connections. There are two technologies to mount components onto PCB: through-hole mount technology (THMT), and surface mount technology (SMT) [7]. Through-hole technology, also spelled "thru-hole", refers to the mounting scheme used for electronic components that involves the use of leads that are inserted into holes drilled in PCBs and soldered to pads on the opposite side [8, 9]. Surface-mount technology is a method for producing electronic circuits in which the components are mounted or placed directly onto the surface of printed circuit boards. Compared to THMT, SMT has many advantages including higher component density, better mechanical performance, higher real-estate rate, and certainly lower cost, so SMT largely replaced THMT in the industry [10]. Details about THMT and SMT components will be given in section 1.2.

1.2 Electronic Components

As mentioned in section 1.1, in electronics manufacturing integrated circuits on a silicon chip are packaged to form an electronic component, which prevents the circuits from mechanical damage and corrosion, as well as provides electrical contacts with the printed circuit board. Based on two component-to-PCB mounting technologies, electronic components belong to two categories: through-hole mount technology components and surface mount technology components.

1.2.1 THMT Components

Through-hole mount technology was developed during the 1950s, and has been replaced by SMT since the 1980s. The basic idea of THMT consists of drilling through-holes (vias) in a PCB, inserting component leads through these holes, and wave soldering the lead to pads on the opposite side of PCB. A typical THMT Component is dual in-line package (DIP). Figure 1.2 shows an example of a DIP, and its side-view.

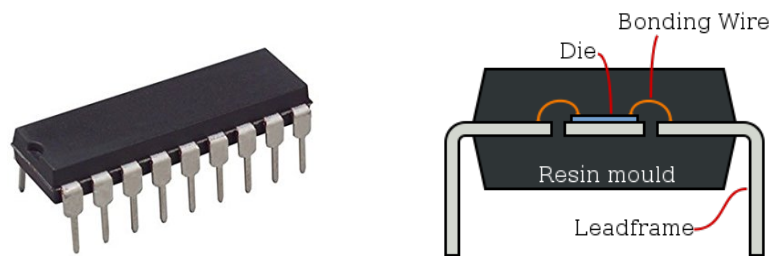


Figure 1.2 A DIP and its side view

An advantage of THMT is the excellent reliability, due to its lead frame structure effectively taking up stresses resulting from thermal expansion in the PCB substrate. In contrast, THMT requires holes to be drilled through the PCB, making the boards more expensive to produce. Also

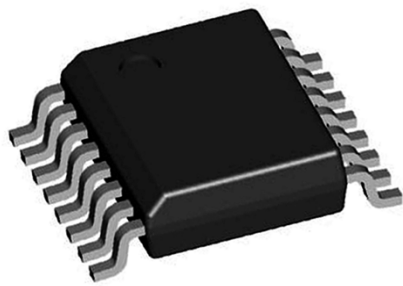
THMT components require more PCB real estate and provide much less I/O, so it has been replaced by SMT component.

1.2.2 SMT Components

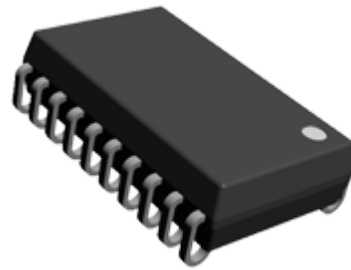
Through-hole mount technology has been widely replaced by surface mount technology since late 1980s. Compared to THMT, SMT mounts or places components directly on the surface of PCB, using a reflow method to form the solder joint [11]. SMT has several design advantages compared to THMT. Components can be placed on both sides of the circuit board since no through-holes are required, which increases the usage of PCB surface area significantly. Also since no holes are needed, SMT has much higher component density and higher density of connections, with lower cost and faster assembly. SMT components are usually smaller, because they have finer lead pitches and I/O can be placed around all four sides of the component. In addition SMT has better mechanical and electrical performance [12]. One disadvantage of SMT is complicated thermal management, since SMT components are small. Also, with less solder for each joint, reliability of solder joints becomes a greater concern [13]. There are a variety of SMT components, and they will be illustrated in the following session.

1.2.3 Leaded Components

There are mainly two types of leaded components: Gull Wing and J-Lead. Figure 1.3 shows the schematic of a Gull Wing component and a J-Lead component.



(a)



(b)

Figure 1.3 Gull Wing component (a) and J-Lead component (b)

From Figure 1.3 it can be noticed that a Gull Wing device is a surface mount component that has its leads folded out from its body in the shape of a 'L', while a J-leaded device is a surface mount component that has its leads folded under its body in the shape of a 'J'. Table 1.1 lists main types of Gull Wing component and J-Lead component [14].

Table 1.1 Main Types of Gull Wing and J-Lead Packages [3]

Gull Wing Components		J-Lead Components	
Small Outline IC (SOIC)		Small Outline J-Lead (SOJ)	
Quad Flat Package (QFP)		Plastic Leaded Chip Carrier (PLCC)	
Small Outline Transistor (SOT)			

1.2.4 No-Leads Components

Besides leaded components, there are also SMT components with bare metal terminations on the bottom of the component to be placed directly onto the solder paste printed on the copper pad of a PCB. Components with no leads are called no-lead components. Typical no-lead components include the surface mount resistor (SMR), and the quad flat no-lead (QFN) component. Figure 1.4 shows illustration of SMR and QFN components.

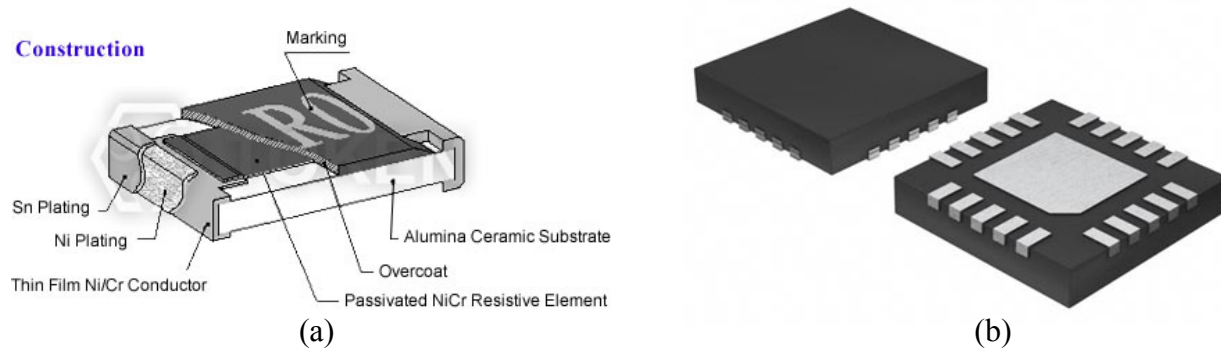


Figure 1.4 SMR component (a) and QFN component (b)

Flat no-leads component is also known as micro leadframe (MLF) and small-outline no-leads (SON). Flat no-lead components usually are plastic encapsulated, in which the die is wire bonded with planar copper lead frame. The copper lead frame forms perimeter lands on the component bottom to provide electrical connections to the PCB. Flat no-lead components are usually square or rectangular in shape, and include an exposed thermal pad at center of the component bottom to improve heat transfer [15]. Figure 1.5 shows the side view of a QFN component.

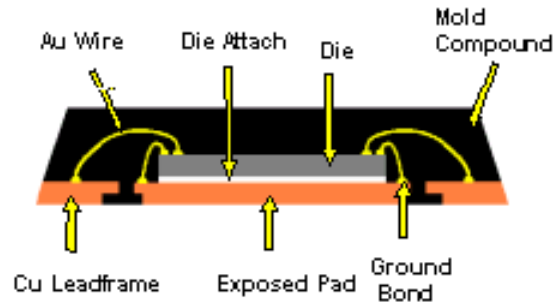


Figure 1.5 Side view of QFN component

The advantages for no-leads components include reduced lead inductance, a small sized (near chip scale) footprint, and low weight. They typically have good thermal and electrical performance. One disadvantage of no-leads components, especially for components with small exposed contacts as well as a large area of exposed thermal pad is that they easily float on the pool of molten solder under the thermal pad during reflow assembly.

1.2.5 BGA (Ball Grid Array)

There is another type of SMT component, which is different from lead and no-lead components, and these components are called area arrays. When the electronic packaging industry had made the transition to surface mount technology, there was no necessary reason that I/O leads must be limited to the perimeter of the component. Instead, I/O can be installed in the type of a full 2-dimensional lattice, or area array, throughout the bottom surface area of the component, providing a much greater number of connections than a lead type component where only the out perimeter is used [16]. Within array area components, the BGA component is the most famous and popular.

Figure 1.6 shows the picture for a BGA component of both the top and bottom side. From the figure one can easily notice that the BGA is a component with one face attached or partly attached with solder balls in a grid pattern for conducting electrical signals between the

integrated circuit and the PCB on which it is mounted. BGA components with attached tiny solder balls are placed on a PCB with copper pads in similar pattern that matches, and electrically connected through a reflow process.

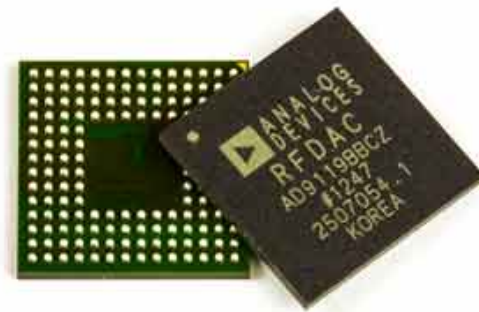


Figure 1.6 Top and bottom side of a BGA component

Compared to leaded components, BGA components can provide higher density I/O, with better thermal management, and lower lead inductance and hence superior electrical performance. Meantime, BGA components are not mechanically compliant, given that the solder balls are not able to be as flexible as longer leads can. Due to coefficient of thermal expansion (CTE) between the PCB and the BGA, exposing a BGA component to a thermal or mechanical harsh environment involving fatigue can cause the solder joints to fail. This reliability issue can be improved by matching the CTE of BGA component and the PCB. A process called underfilling, which injects an epoxy mixture material under the BGA after it is soldered onto the PCB, can help improve the mechanical stability of BGA component.

There are a number of types of BGA components [17]:

1. PBGA – Plastic Ball Grid Array: can be either 2 layer or 4 layer substrates, with organic materials, with a variety of BGA pitch size and component body size. Figure 1.7 shows a typical cross-section of PBGA component mounted on PCB.

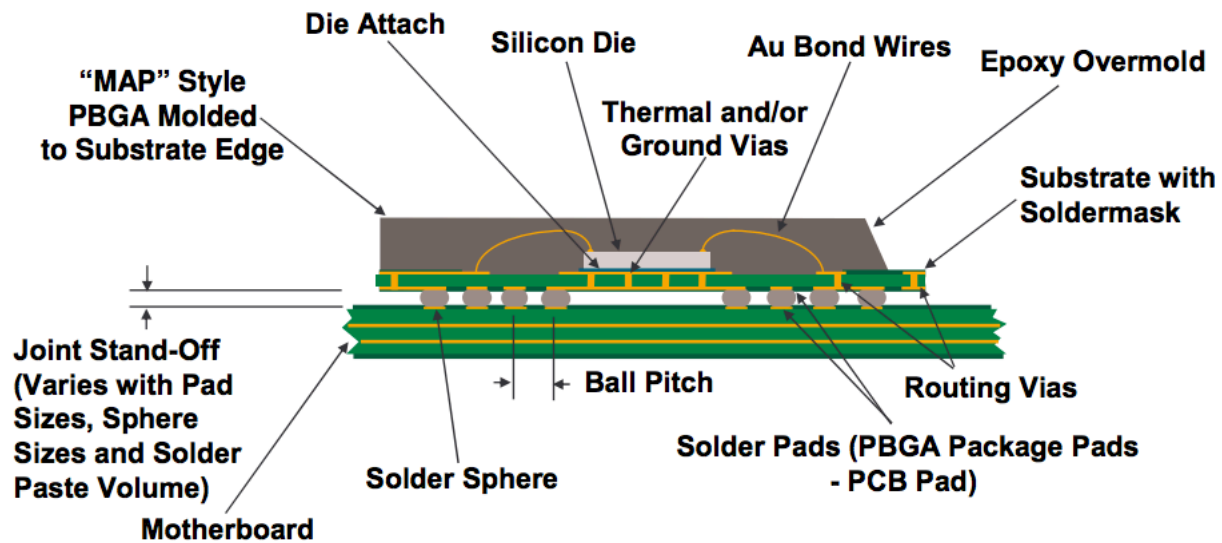


Figure 1.7 Cross-Section view for a PBGA component

2. CBGA – Ceramic Ball Grid Array: uses a multi-layer ceramic substrate. Figure 1.8 shows a schematic of cross-section of a CBGA component, with a flip-chip attached silicon die, and an underfill.

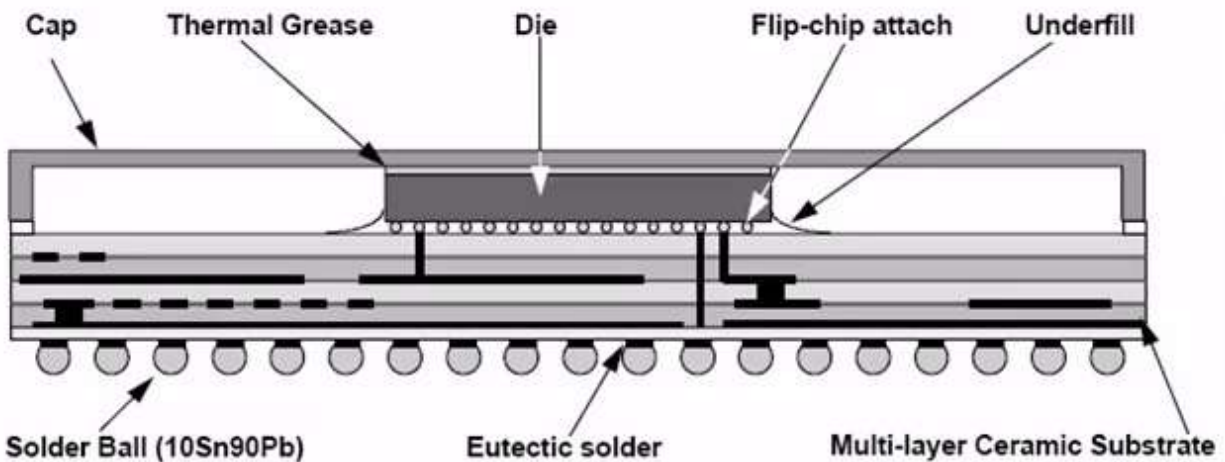


Figure 1.8 Cross-Section view for a CBGA component

3. FCBGA – Flip-Chip BGA: uses direct electrical connection of face-down (or flipped) IC dies onto substrates or carriers, using conductive bumps on the bond pads of the chip surface, as

shown in Figure 1.8. A FCBGA can either use plastic or ceramic substrate with multiple layers. Advantages of flip-chip includes reduced electrical inductance, and component footprint, along with higher die shrink.

4. TBGA – Tape Ball Grid Array: contains a substrate composed by 1-2 band-shape of soft-layer material. Figure 1.9 shows a schematic of cross-section of TBGA Component.

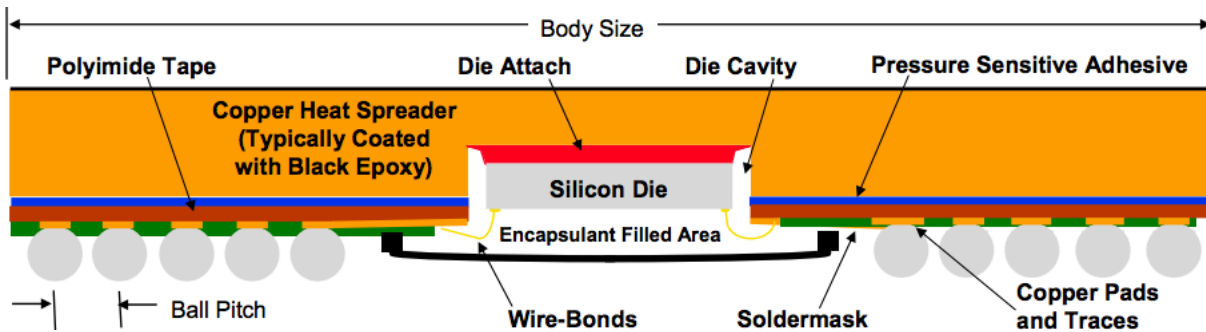


Figure 1.9 Cross-section view for a TBGA component

5. CDPBGA – Cavity Down Plastic Ball Grid Array: uses a cavity down wire bonding configuration, resulting in a concave area in the center. Figure 1.10 shows a comparison of a PBGA with a standard (cavity up) configuration and cavity down configuration of wire bonding.

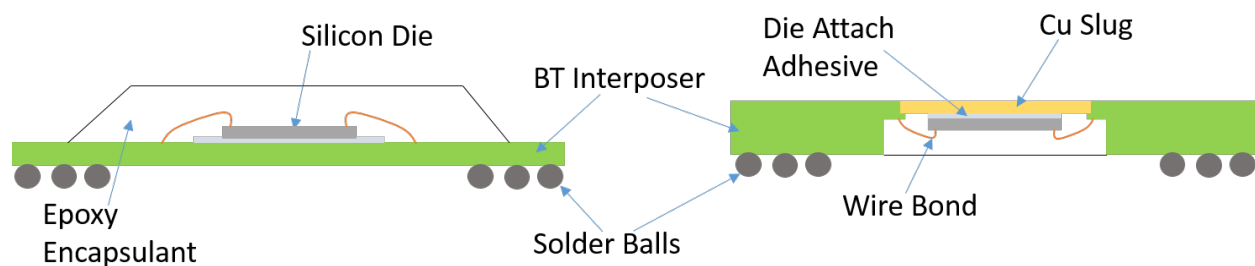


Figure 1.10 Cross-section view for a standard BGA (left) and cavity down BGA (right)

6. CSP - Chip-Scale Package: a BGA component that has an area of no greater than 1.2 times than that of the die and it must be a single-die, direct surface mount component, with a ball pitch of 1mm or less. Figure 1.11 shows comparison of a standard BGA Component with a CSP.

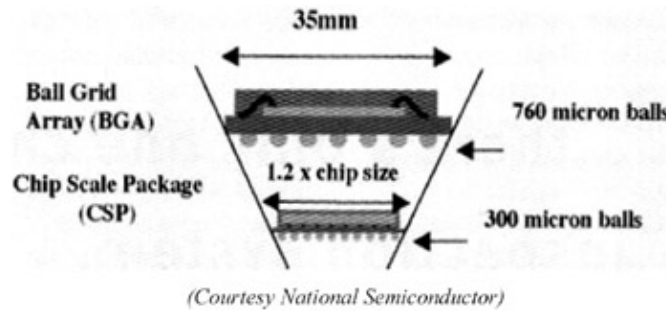


Figure 1.11 Comparison of a standard BGA (top) and a CSP (bottom)

1.2.5 PGA (Pin Grid Array)

Pin Grid Array (PGA) is another type of array area component. Similar to a BGA Component which uses attached solder balls at bottom surface, PGA components use regular arrayed pins for electrical signal conduction. Figure 1.12 shows a PGA component in the Motorola 68020 microprocessor.

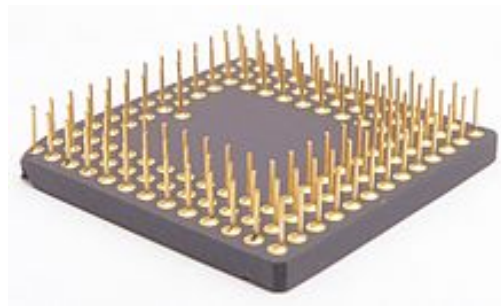


Figure 1.12 A PGA component used in Motorola 68020 microprocessor

PGA components are mounted on a PCB using the through hole method or inserted into a socket. Compared to a traditional DIP, a PGA allows for more I/O. There are different types of PGAs, including Plastic Pin Grid Array (PPGA), Flip-Chip Pin Grid Array (FCPGA), Ceramic Pin Grid Array (CPGA), and Organic Pin Grid Array (OPGA).

1.2.5 LGA (Land Grid Array)

Land Grid Array (LGA) is another type of area array component. Similar to solder balls with a BGA component and pins with a PGA component, an LGA component has rectangular flat contacts on the underside of the package. Compared to PGA components which can only be mounted on a PCB by inserting the component into a socket or through hole, LGA components can be electrically connected to a PCB with same type of contacts, by using a LGA socket or by soldering directly to the board with solder paste. Figure 1.13 shows a schematic comparison of PGA, LGA, and BGA components.

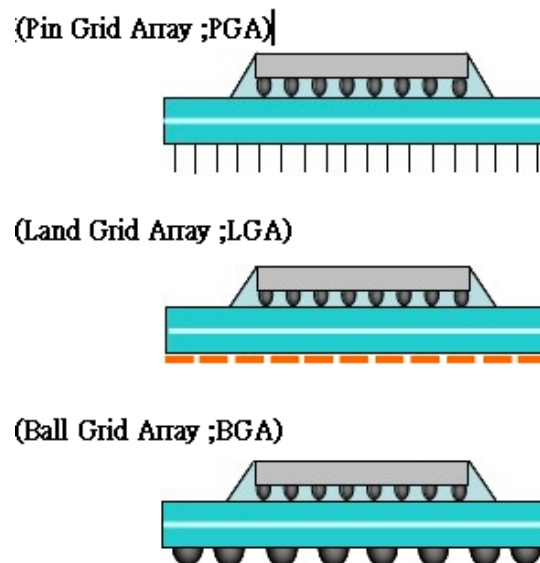


Figure 1.13 Schematic comparison of PGA (top), LGA (middle), and BGA (bottom)

1.3 Substrate for Electronic Packaging

As we mentioned the hierarchy of interconnection levels in electronic packaging, Level 2 is comprised of connections from component to component, or to an external connector, which is called a printed circuit assembly (PCA). A PCA is based on a substrate, usually called a PCB. The PCB provides mechanical support, thermal dissipation, as well as electrical connections to

components [18]. A PCB consists of a non-conductive substrate, on which conductive traces, pads and other features etched from copper sheets are laminated. PCBs can be single sided, double sided, with multi-layers of laminated substrate. Conductive parts on different layers are electronically connected with each other through vias. A via can be either a hole through the board, or it can be a blind via that is exposed only on one side of the board, and sometimes a buried via is used to connect internal layers without being exposed on either surface [19]. Figure 1.14 shows a cross-section view of a PCB with all three types of vias.

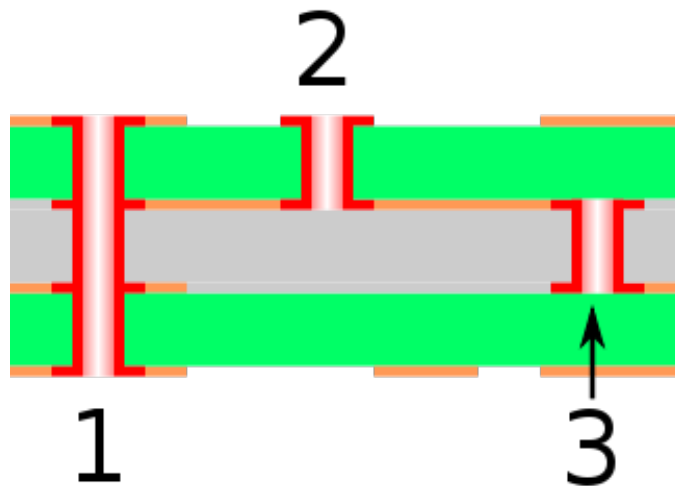


Figure 1.14 Cross-section view of a PCB with different types of vias: (1) through hole; (2) blind via; (3) buried via. The green and gray layers are non-conducting, while the thin orange layers and vias are conductive.

1.3.1 Substrate Material

For substrate materials, FR-4 is widely used. FR-4 is a composite material composed of woven fiberglass cloth with an epoxy resin binder that is flame resistant. “FR” stands for flame retardant, and type “4” indicates woven glass reinforced epoxy resin [20]. FR-4 glass epoxy is a good electrical insulator with considerable mechanical strength, in both dry and humid environments.

Table 1.2 summaries engineering properties of FR-4.

Table 1.2 Engineering properties of FR-4

Key Characteristics	Test Method	Units - English (SI)	Typical Values
Tensile Strength (0.125") LW	ASTM D638	ksi (MPa)	62 (430)
Compressive Strength, Flatwise (0.500")	ASTM D695	ksi (MPa)	66 (455)
Flexural Modulus (0.062") LW CW	--	ksi (GPa)	2,900 (20) 2,600 (18)
Shear Strength (punch type, 0.062")	ASTM D732	psi (MPa)	21,500 (148)
Coefficient of Thermal Expansion	--	" / °C x 10 ⁻⁶	15
Temperature Index	--	°C	130
Glow Wire Flame Index & Ignition Temperature	IEC 60695-2-12	°C	960
Hot Wire Ignition	UL 746A	Sec	120
High Current Arc Ignition (3mm)	UL 746A	Arcs	120
Arc Resistance (0.125")	ASTM D495	Sec	140
Comparative Tracking Index (.125")	ASTM D3638*	V	230
Dielectric Strength Condition A	ASTM D149	V/mil	635
Volume Resistivity (0.062")	ASTM D257	Ω – cm	3(10) ¹⁵
High Voltage Arc Resistance	UL 746A	Sec	300
High Voltage Arc Tracking Rate	UL 746A	mm/min	0

The copper layer thickness of FR-4 is typically denoted using “weights” such as “half-ounce” or “one-ounce”. This represents the weight of copper over a 1ft² area used in the substrate. Therefore a “one-ounce” copper layer FR-4 will be about 34 microns or 1.34 mils thick [21]. From Table 1.2 it can be found that the coefficient of thermal expansion (CTE) of FR-4 laminate is about 15 ppm/°C. The CTE of a PCB can be affected by the number of metal layers, laminate materials, trace density, operating environment and other considerations. FR-4 has a glass transition temperature (T_g) ranges from 120°C to 180°C, when the resin changes from a glassy to a plastic state. The recommended operating temperature for FR-4 is typically below 130°C [22, 23]. Besides FR-4, the standard epoxy glass substrate and bismaleimide triazine (BT) are other common materials for PCB substrate.

1.3.2 Solder Mask

In order to protect the copper traces on the surface of a PCB against oxidation, and also prevent solder bridges forming between closely spaced solder pads, a thin lacquer-like layer of polymer is applied, which is called solder mask. Acrylic and epoxy polymers are commonly used materials for solder mask. There are two kinds of solder mask designs for a PCB, which are solder mask defined (SMD) and non-solder mask defined (NSMD). For a NSMD, the copper pad on the surface of the PCB (to which a component BGA solder ball is attached) is smaller than the solder mask opening, while for SMD the solder mask opening is smaller than the copper pad.

Figure 1.15 below shows difference between NSMD and SMD PCB designs.

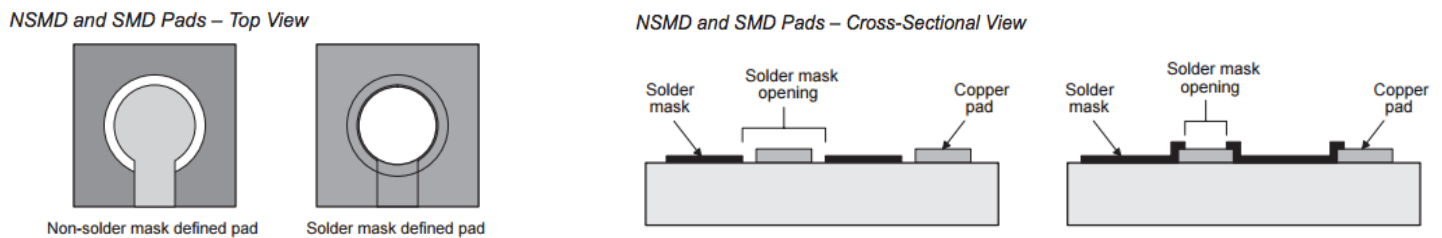


Figure 1.15 Top view (Left) and cross-section view (right) of NSMD versus SMD PCB

Figure 1.15 shows for a NSMD-configured PCB, there is a gap between the solder mask and the circular copper pad. With this configuration, the solder flows over the top surface and the sides around the copper pad. This additional NSMD soldering area results in a stronger mechanical bond. So NSMD PCB design has been proven to have higher resistance to thermal-mechanical fatigue failure because the design geometry generates less stress concentration. As a result NSMD is more widely used as a standard for the PCB design by the industry.

1.3.3 Surface Finish

Since solder mask can only be used to protect copper traces and cannot be extended to cover copper pads on the PCB, an additional surface finish is required to be applied over the exposed copper pads area. The surface finish is sometimes called surface plating or coating. Besides protecting copper pads from corrosion and oxidization, surface finish can also increase solderability of solder paste to the copper pad, by dissolving the outermost layer of surface finish during reflow or wave soldering. Sometimes surface finishes are considered solder mask over bare copper (SMOBC). Figure 1.16 shows a schematic of cross-section view of PCB with a surface finish on top of copper pad.

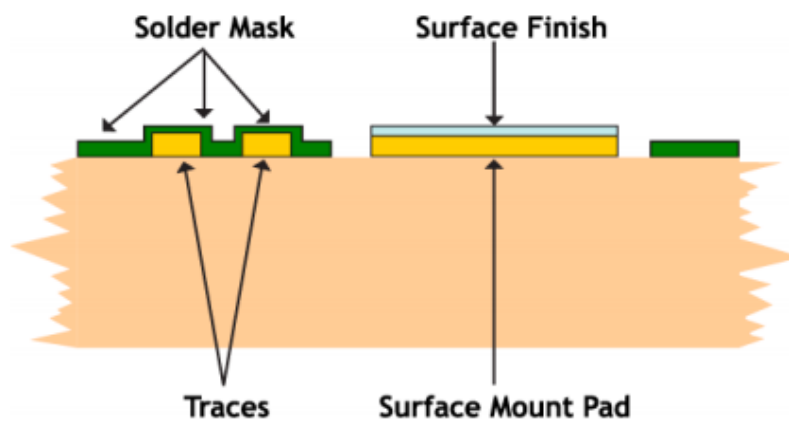


Figure 1.16 Cross-section view of a PCB with surface finish applied on copper pad

There are several different types of surface finishes [24]:

1. Hot Air Solder Leveling (HASL): has been the predominant surface finish used with tin-lead (SnPb) solder for a long time. This process consists of immersing the PCB into a molten tin-lead or Lead-Free solder bath. Then solder will cover any exposed metal surfaces on the PCB without a solder mask on it. After the board is pulled out of the solder bath, hot “air knives” are used to remove excess solder, which leaves only a layer of coating on the copper pad surface. HASL is

one of the least expensive surface finishes available, and has excellent solderability. However, flatness or coplanarity of the coated HASL surface is very poor, and the PCB is susceptible to thermal shock damage during the process. Therefore, the popularity of HASL has fallen significantly in recent years.

2. Organic Solderability Preservative (OSP): is an organic compound-based coating using a thin protective layer of carbon-based organic compound over the copper pad to prevent it from oxidation and contamination. OSP finish is the leader in low cost surface finishes, and has superior co-planarity and solderability. Disadvantages of OSP finish include poor shelf life (less than 6 months), easy degradation with temperature, handling sensitivity, and difficulty during circuit testing because the coating is non-conductive.

3. Immersion Tin (ImSn): another finish that is ideal for a flat surface finish. ImSn surface finish will form a tin/copper (SnCu) intermetallic joint during the surface deposition process and will continue to grow, resulting in significant shortening of the shelf life. Also during wave soldering, when exposed to elevated temperature, the thin tin layer often can almost completely be converted to a SnCu intermetallic, leading to very poor solderability. Another significant problem with ImSn is that it uses thiourea, which is carcinogen.

4. Immersion Silver (ImAg): is a recent addition to the list of surface finish options and continues to grow in popularity. ImAg is a preferred surface finish for those concerned with excellent solderability, long shelf life, and easy probe testing. It performs favorable reliability in thermal and mechanical testing. It can generate a “creep corrosion” problem when using ImAg in an environment involving high sulfur and humidity.

5. Electroless Nickel Immersion Gold (ENIG): is a two-layer metallic coating over catalyzed copper, with nickel (Ni) layer acting as a diffusion barrier to the copper pad and surface to which

the soldering occurs, covered by a gold (Au) layer which protects the nickel from oxidation during storage. ENIG provides excellent shelf life, good wettability, great coplanarity for fine pitch components, easy in-circuit testing, and certainly improved product reliability. The only concern when using ENIG surface finish is it's higher per unit cost.

6. Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG): depositing additional electroless palladium layer to ENIG over the nickel layer and below gold layer. This palladium layer can prevent possible contamination of the nickel migrating into the gold, which can eliminate the “black pads” phenomenon for the ENIG surface finish and thus increasing reliability. However, ENEPIG is more expensive than the already costly ENIG surface finish, especially a concern for those on a tight budget.

In summary, choosing right PCB surface finish is essential for predicting cost, quality, and reliability of any printed circuit assembly. Each surface finish has its strength as well as weakness to consider when matching it with your particular needs. Table 1.3 below shows a conclusion of all surface finishes mentioned within this section.

Table 1.3 Summary of properties of surface finishes

Type	Planarity	Solderability	Al Wire Bondable	Au Wire Bondable	Contact Surface
HASL	POOR	GOOD	NO	NO	NO
LFHASL	FAIR	GOOD	NO	NO	NO
OSP	GOOD	GOOD	NO	NO	NO
IMM Ag	GOOD	GOOD	YES	NO	NO
IMM Sn	GOOD	GOOD	NO	NO	NO
ENIG	GOOD	GOOD	YES	NO	YES
ENEPIG	GOOD	GOOD	YES	YES	YES
Elec Au	GOOD	GOOD	YES	(soft only)	YES

* Finish cost factor only, all other features being equal.

1.4 Solder Alloy

From Section 1.1, in Level 2 of the hierarchy of interconnection levels for electronic packaging, the components are attached to the PCB substrate using solder joints, which are melted metal alloys providing permanent metallurgical bond between the component and the PCB to form electrical, mechanical, and thermal connections [25]. Alloys are mixtures of two or more metal elements, in a well-controlled process to produce desirable properties. Soldering is the metallurgical joining process in which the components and PCB substrate are joined by heating the filler material, called the solder [26, 27]. Solder usually has a melting point range of 90°C to 450°C, which should be lower than the damage threshold of the components and PCB substrate that are intended to be joined, to prevent damage [28]. During soldering process, an intermetallic compound (IMC) layer will be formed at the connected surface between the solder joint of the component and the PCB substrate, which actually provides the metallurgical bonding. Because the IMC layer is brittle, the thickness of the layer must be controlled. Solder alloys must have good properties in order to accomplish their function, keeping the interconnection to maintain good electrical, mechanical, and thermal reliability. The properties to be considered for solder alloy selection are summarized in Table 1.4.

Table 1.4 Summary of properties to be considered for solder alloy selection [25]

Manufacturing	Reliability
Melting/liquidus temperature	Electrical conductivity
Wettability (of copper)	Thermal conductivity
Cost	Coefficient of thermal expansion
Environmental friendliness	Shear properties
Availability and number of suppliers	Tensile properties
Manufacturability using current processes	Creep resistance
Ability to be made into balls	Fatigue properties
Copper pick-up rate	Corrosion and oxidation resistance
Recyclability	Intermetallic compound formation
Ability to be made into paste	

1.4.1 Tin-Lead Solder

The most popular and favorite solder alloy in history is tin-lead (SnPb) solder, which can be dated back to thousands of years ago to the ancient Romans. For electronics manufacturing industry, the eutectic tin-lead solder with 63% tin and 37% lead (63Sn37Pb) by weight is the most universal option. The 63Sn37Pb is called to be “eutectic” because the melting point of the solder is the same as its freezing point. A eutectic alloy has single temperature above which the entire alloy is in pure liquidus state, and below which the alloy will become pure solidus. Not all

alloys have a eutectic point. Usually a non-eutectic alloy has only a “pasty range” of temperature, within which the alloy is partially solid and partially liquid [29, 30]. Eutectic 63Sn37Pb allows for a more controlled soldering process. The melting temperature for 63Sn37Pb is about 183°C, which is low enough to form a good metallurgical bond without bringing thermal damage to the component and PCB substrate. Figure 1.17 shows the phase diagram of a tin-lead alloy.

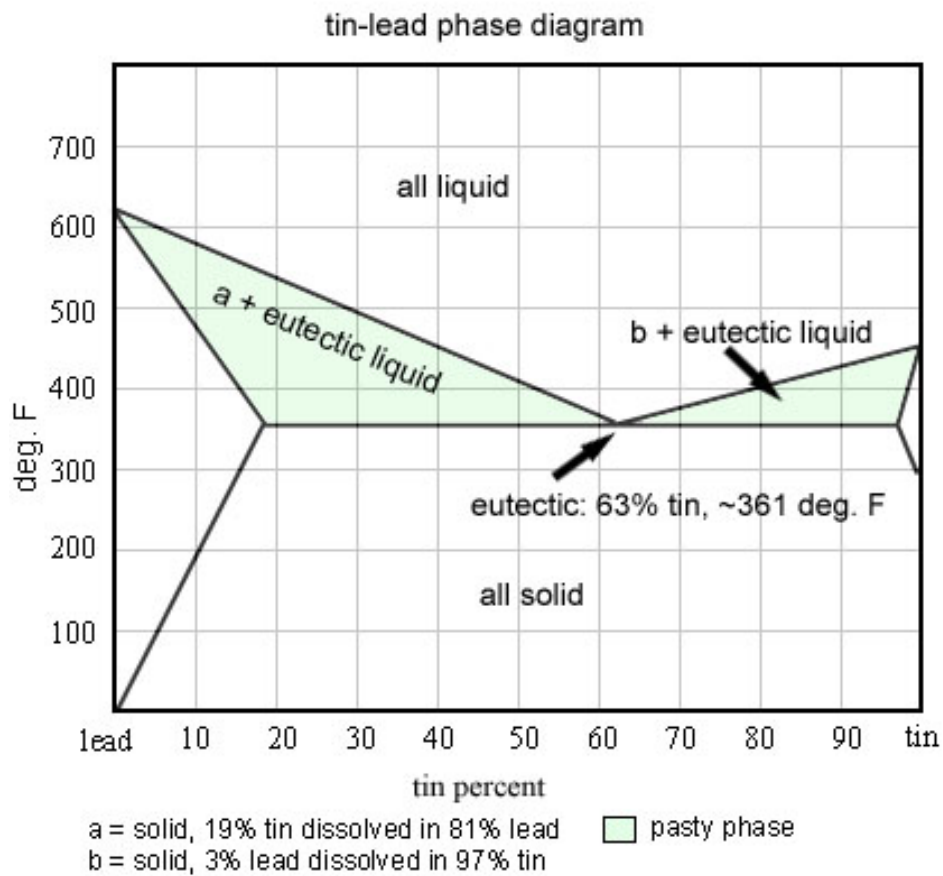


Figure 1.17 Phase diagram for tin-lead solder alloy

63Sn37Pb has many advantages, including eutectic composition with low melting point, low cost, good wetting and manufacturability, excellent electrical conductivity, and adequate fatigue

resistant [31, 32]. So 63Sn37Pb can provide good mechanical, electrical, and thermal performance, as well as maintain great reliability.

1.4.2 Lead-Free Solder

Despite having many advantages, unfortunately 63Sn37Pb solder has a big disadvantage that lead (Pb) is a highly poisonous metal, which can cause harmful health issues to organ and nervous system of humans including anemia, cardiovascular disease, mental retardation, and learning disabilities [33, 34]. Since the 1990s, international legislation has been adopted to limit the use of lead in electronics. For examples in Japan the advisory committee of Japan Institute of Electronics Industry Development Association (JEIDA) proposed a roadmap in 1998 for commercialization of lead-free solders. In the European Union, the Waste of Electrical and Electronic Equipment (WEEE) have forced all electronics in Europe to remove lead completely by 2008, and the Directive of the Restriction of the Use of Certain Hazardous Substances (RoHS) prohibits the use of lead in electrical components manufactured after 2006 [35, 36]. In the United States, governmental organizations like the Occupational Safety and Health Administration and National Institute for Occupational Safety and Health have set permissible exposure limit for lead exposure in the workplace.

Due to these regulations, the electronics manufacturing industry has been searching for a successor to replace tin-lead solder, called lead-free solder [37]. Some properties for lead-free solders are [38]:

- Low melting temperature similar to 63Sn37Pb
- Good wettability closed to 63Sn37Pb
- Low cost
- Adequate availability on Earth

- Compatibility with soldering process
- Material properties similar or better than 63Sn37Pb (CTE, ductility, thermal and electrical conductivity, etc.)
- Environmental friendship

Eventually, most researchers make the lead-free transition from tin-lead solder by adding traces of metal elements into Sn-based solders. These elements include copper (Cu), silver (Ag), bismuth (Bi), indium (In), zinc (Zn), antimony (Sb), and others. Tin is selected as a major component and base element for solder alloy because of its excellent ability to form intermetallic compounds with a number of other metals. Among all these lead-free solder alloys candidates, the tin-silver-copper solder alloys family, or simply “SAC” alloys, are widely used. SAC alloys are near eutectic with melting temperatures range between that of pure tin (232°C) and 63Sn37Pb (183°C). They can also provide adequate thermal fatigue properties, strength, and wettability. Typical SAC alloys contain 3–4% silver (Ag), 0.5–0.7% copper (Cu), and the balance 95%+ tin (Sn) [39, 40]. For example, the commonly used "SAC305" solder consist of 3.0% silver and 0.5% copper. Cheaper alternatives with less Silver are used in some applications, such as SAC105 and SAC0307 (0.3% silver, 0.7% copper), at the expense of a somewhat higher melting point. The following are some examples of SAC-family solders:

- SAC305 (Sn96.5Ag3.0Cu0.5): most popular SAC solder alloy, especially in the automotive and consumable electronics industries. Pasty melting range around 217°C to 220°C. Falls under the JEIDA recommendation for lead-free soldering. Low cost, excellent fatigue resistance, good mechanical characteristics, best wetting SAC alloy.

- SAC105 (Sn98.5Ag1.0Cu0.5): popular in automotive manufacturing industry, most commonly for cellphone industry, because of superior drop and vibration resistance. Pasty melting range around 220°C to 225°C. Low cost.
- SAC405 (Sn95.5Ag4.0Cu0.5): contains more silver. Sometimes better thermal fatigue resistance. More expensive than SAC305.
- SAC387 (Sn95.5Ag3.8Cu0.7): recommendation of the European IDEALS Consortium. Not commonly used in the United States.
- SAC396 (Sn95.5Ag3.9Cu0.6): recommendation of the U.S. NEMI group. Used in the United States occasionally.
- SnCu Eutectic (Sn99.3Cu0.7): eutectic mixture of tin and copper. Eutectic melting point to be 227°C. Low cost, but poor mechanical properties, and easy to have tin whiskers.
- SnAg Eutectic (Sn96.5Ag3.5): eutectic mixture of tin and silver. Eutectic melting point to be 221°C.

1.4.3 New Solder Alloy and Solder Doping

Both industry and academia are undergoing research projects on other different kinds of Sn-based lead-free solders, by adding traces of metal elements such as bismuth (Bi), indium (In), zinc (Zn), antimony (Sb), and others. Some examples of these non- SAC family solders include:

- 42Sn58Bi Eutectic: tin-bismuth eutectic mixture with a melting temperature at 138°C. This solder alloy provides a low melting temperature, which can reduce thermal damage. Bismuth content can increase the mechanical strength. For high temperature application the melting point maybe too low. Also availability of bismuth is a concern.

- 48Sn52In Eutectic: tin-indium eutectic mixture with a melting temperature at 118°C. This solder alloy provides even a lower melting temperature than 42Sn58Bi. But at the same time indium content will decrease the mechanical strength, and availability of indium makes this solder alloy to be expensive.
- 20Sn80Au Eutectic: tin-gold eutectic mixture with a melting temperature at 280°C. This particular alloy of gold tin (AuSn) is considered a solder because it has a melting point lower than the 350°C transition temperature into braze materials. The hardness of 20Sn80Au is high, making it much more rigid than other solders, which at same time generates some unique manufacturing difficulties. The cost is high because of low availability of gold.
- 95Sn5Sb: tin-antimony non-eutectic solder alloy with a pasty range of 232-240°C. It can be used in high temperature applications. Strength and hardness increases with antimony content. 95Sn5Sb has a good thermal fatigue performance. However, wetting properties are poor. The toxicity of antimony is also a potential concern.
- 91Sn9Zn: Tin-zinc eutectic mixture with a melting temperature at 199°C. Strength and temperature increases with zinc content. However, this solder alloy has wetting problem and corrosion issues because zinc is prone to oxidation.

Another method in the development of new solder alloy is called solder alloy addition, or solder micro-alloying, or solder doping. Similar to semiconductor industry, doping here means adding dopants to traditional eutectic or non-eutectic solder alloy to form new solder alloy. This doping idea is inspired by the “impurities” involved during soldering assembly. The terminology of doping here is slightly different with that being used in semiconductor industry, where the content of dopant is limited to be less than 1%. For new solder alloy development, the dopant

level can be a large amount. In the literature solder doping refers to adding dopant into SAC solder pastes, forming a new doped solder alloy in the term of SAC+X, where X stands for the dopant. Typical dopants used include Bi, In, Ni, La, Mg, Mn, Ce, Co, Ti, Zn, etc. [41]. Research shows that doped solder alloy can enhance shock/drop reliability, wetting, and other properties. For example, researchers have shown that the addition of bismuth (Bi) as a dopant has been demonstrated to have several beneficial effects, including improvements in shear strength and reductions of IMC layer thickness in lead-free solder materials [42].

Figure 1.18 demonstrates market share of different lead-free solder alloys (a), and different SAC solder alloys (b).

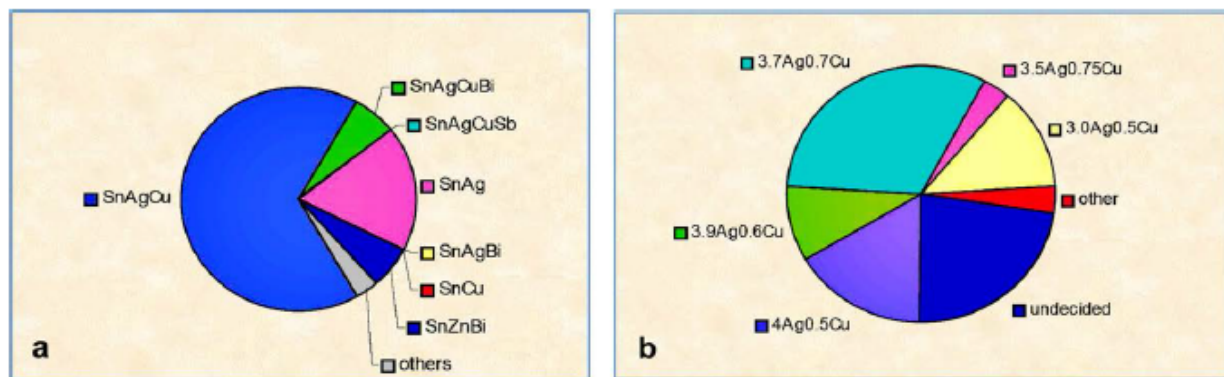


Figure 1.18 Market share of lead-free alloys (a) and SAC alloys (b)

1.5 SMT Assembly Process

In electronic packaging, electronic components are attached on copper pads of PCB substrate through the SMT assembly process. SMT assembly is the central part of entire SMT packaging technology [43]. Figure 1.19 shows a typical SMT assembly process flow.

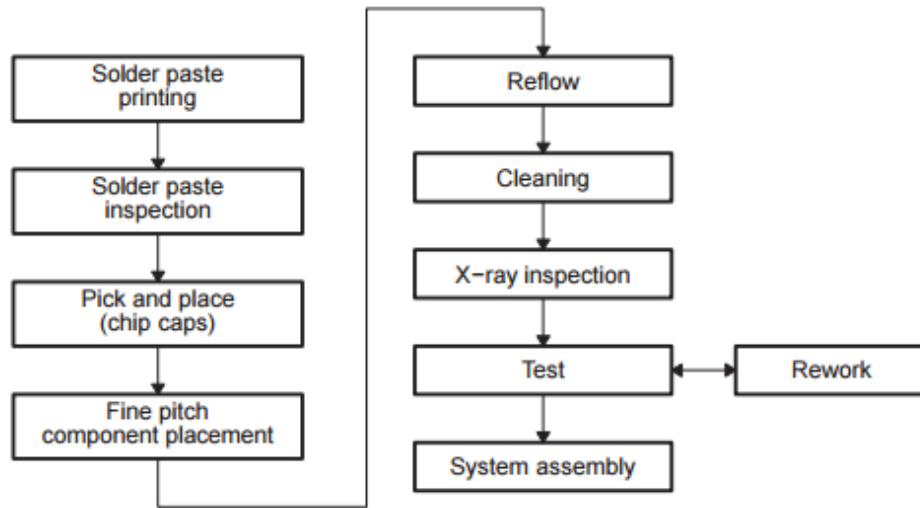


Figure 1.19 Typical SMT assembly process flow

From Figure 1.19, it can be concluded that SMT assembly process involves the following major steps:

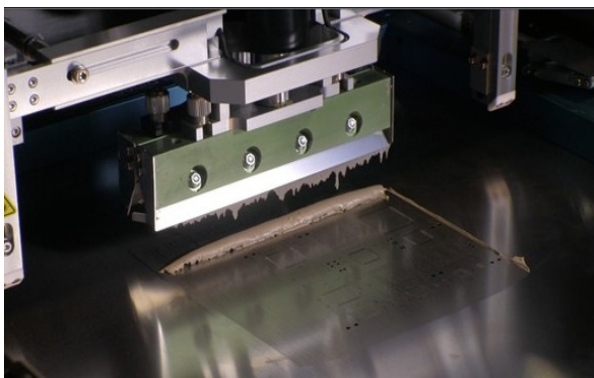
- Step 1: Printing solder paste: the first principal step in SMT Assembly. During this step solder paste is printed onto the copper pads of the PCB, to be prepared to hold SMT components in place before reflow soldering. Solder paste consists of powder of metal particles suspended in a thick medium called flux. Flux acts as a temporary adhesive to hold the components until the solder paste melts during reflow process and makes a metallurgical bond. Solder paste is sticky, with an appearance that looks like a toothpaste.

Figure 1.20 shows a picture of solder paste.

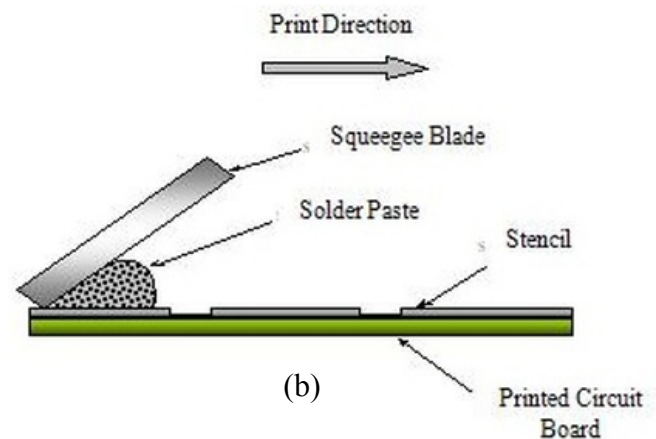


Figure 1.20 A picture of solder paste

Solder paste is applied on the copper pads of a PCB substrate surface through the use of a stencil. A stencil is a thin sheet of material (typically stainless steel) with a series of apertures (holes) cut into it, which correspond to the pads on a PCB. The aim for stencil printing process is to accurately deposit the correct amount of solder paste onto the copper pads on the PCB surface so that the solder joint between PCB and component terminal are acceptable with regard to the desired electrical performance and mechanical strength. The most common method of applying solder paste to a PCB using a stencil printer is squeegee blade printing. The squeegees are the tools used to apply the necessary force required to move the solder paste across the stencil and on to the PCB. They are usually made from metal but can also be made from polyurethane. Figure 1.21 shows a picture of stencil printer (a) and cross-section view of a squeegee printing solder paste on stencil.



(a)



(b)

Figure 1.21 A picture of stencil printer (a) and cross-section view of a squeegee printing solder paste on stencil

Key parameters of an effective solder paste print process include squeegee speed, squeegee pressure, stencil separation speed, stencil cleaning, stencil and squeegee condition, print stroke, storage, handling, and inspection.

The quality of stencil printing process is verified by solder paste inspection. A 2D inspection process checks the area of the paste deposit, and a 3D inspection checks the volume of the paste deposit. Figure 1.22 shows an example of fault found by 2D inspection. Figure 1.23 shows different types of unsatisfied printing results.

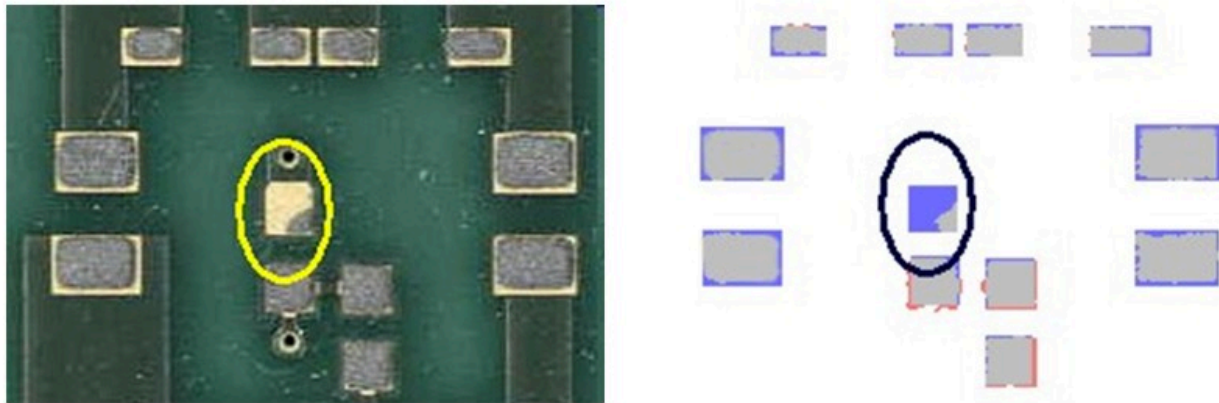


Figure 1.22 Example of fault found by 2D inspection

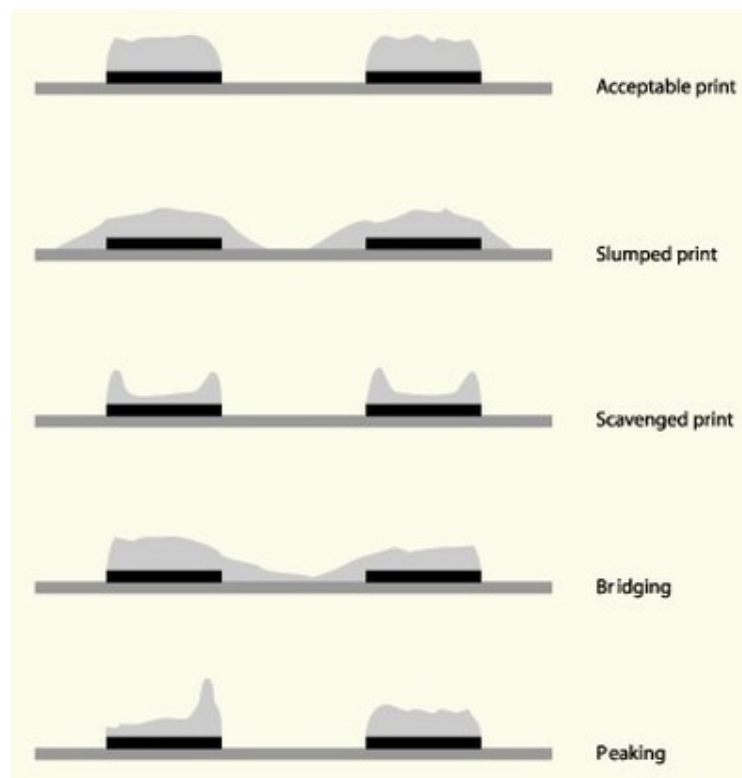
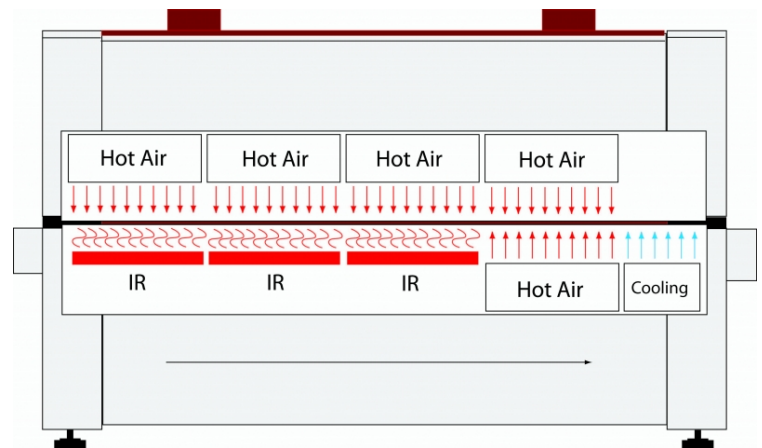


Figure 1.23 Different types of unsatisfied printing result

- Step 2: Component pick and placement: uses automatic machines to pick appropriate SMT components and then place them on the associated copper pad with solder paste printed on the surface of PCB substrate. Component pick-and-place machines are differentiated by a lot of variables including placement speed and accuracy, the type of feeders, serviceable board sizes, mechanical action, inspection capabilities, customer surface, cost and many others [44].
- Step 3: Reflow soldering process: when the entire SMT assembly is subjected to controlled heat through a reflow oven to melt the solder joint and form permanent metallurgical bond between SMT components and copper pad on the surface of PCB substrate. Primarily soldering uses a reflow oven, either infrared or convection, which contains multiple zones and can be individually controlled for temperature. The PCB assembly moves through the zones in the oven on a conveyor belt, and is therefore subjected to a controlled time-temperature profile [45]. Figure 1.24 shows an example of a reflow oven (a) with its cross-section view of structure inside (b),



(a)



(b)

Figure 1.24 (a) Example of a reflow oven (b) with its cross-section view of structure

The reflow soldering process is controlled by a time-temperature thermal profile to form an appropriate metallurgical bond between component and PCB substrate without overheating and thermal damaging the assembly. Figure 1.25 shows a typical reflow thermal profile.

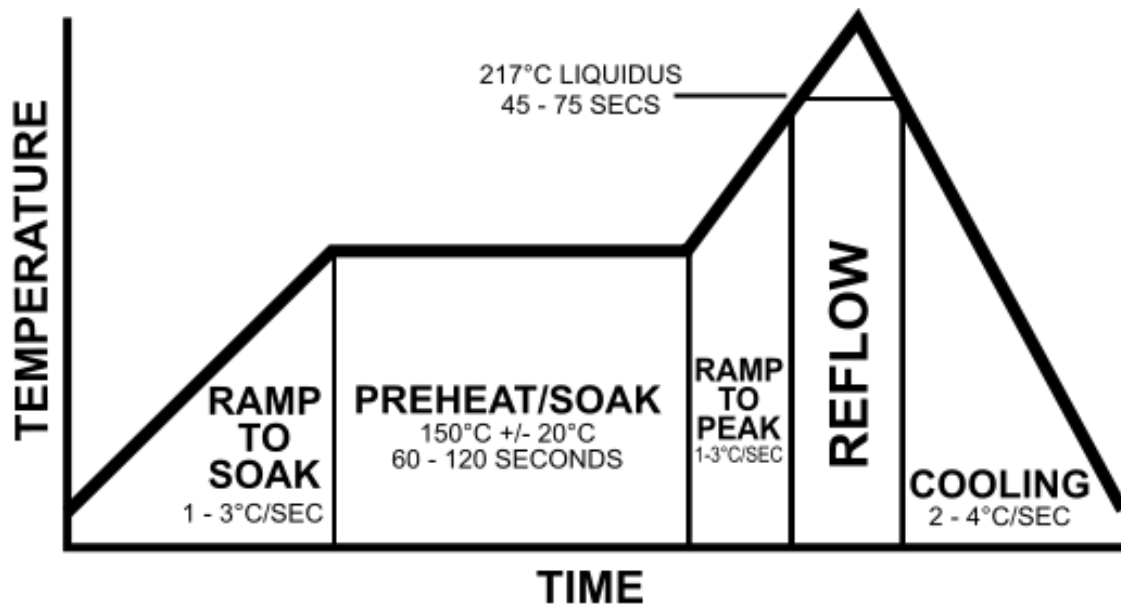


Figure 1.25 A typical reflow thermal profile

From Figure 1.25, it is known that a typical reflow profile contains following stages [46]:

1. Preheat: during this phase the entire SMT assembly are heated to a target soak or dwell temperature with a slow rate (usually no more than 2°C/second). Heating too quickly can cause defects such as cracked components and splattered solder paste.
2. Soak: to ensure all components are up to the required temperature before entering the reflow stage, to remove solder paste volatiles, and to activate the fluxes. Soaks usually lasts for between 20 and 120 seconds. At the end of the soak zone a thermal equilibrium of the entire assembly is desired.
3. Reflow: also referred to as the “time above liquidus” (TAL), where the temperature of the reflow oven is increased above the melting point of the solder paste causing it to form

a liquid. The time the solder is held above its melting point is usually 30 to 60 seconds to ensure correct wetting of the solder paste. The peak temperature during the reflow should be controlled to prevent component failure and other defects.

4. Cooling: the stage during which the assembly is cooled to solidify the solder joints. A common recommended rate of cooling should not exceed 4°C/second.

- Step 4: inspection and testing: X-Ray inspection or automated optical inspection (AOI) is performed to avoid defects in the soldering process [47]. Areas to be checked by AOI process include component presence, polarity, presence of solder, dry joints, solder shorts, and so on. Mechanical and electrical tests for the final entire SMT assembly are conducted to assure the quality of the soldering process.

In summary, Figure 1.26 shows a schematic for a typical SMT Assembly production line.

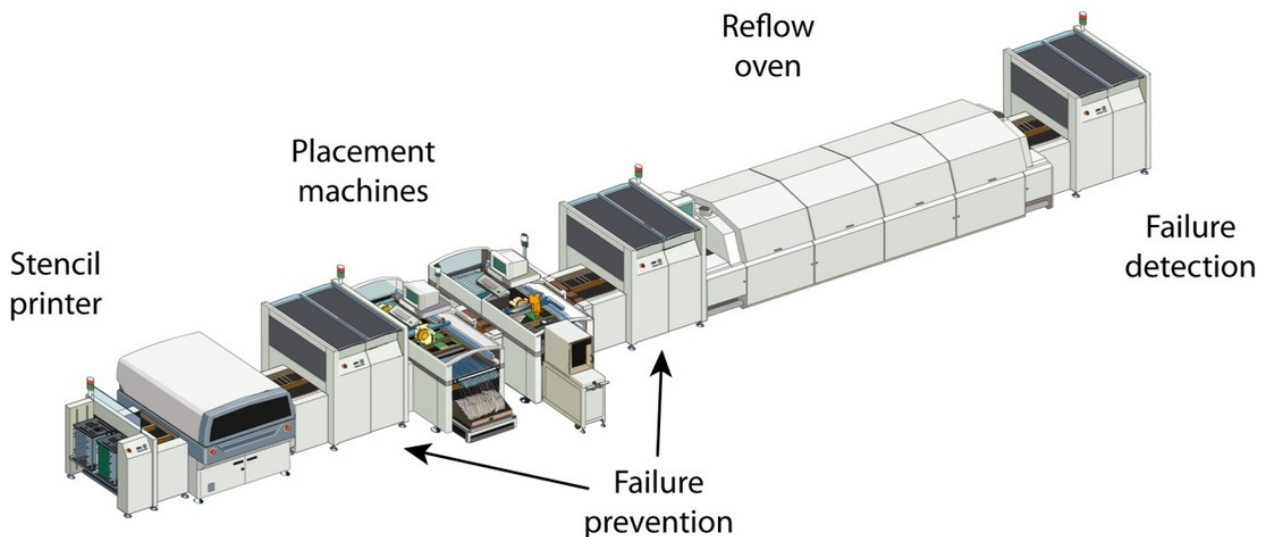


Figure 1.26 A typical SMT assembly production line

1.6 Outline of the Proposal Dissertation

This dissertation contains the following chapters:

- Chapter 1: General Introduction
- Chapter 2: Literature review on the reliability of lead-free assembly, microstructural changes of solder joints, reliability testing including thermal aging and cycling test, vibration and drop test, and solder doping.
- Chapter 3: Description of test vehicle, SMT assembly process, and experimental setup.
- Chapter 4: Reliability data analysis including failure percentage table and 2-parameter Weibull plots
- Chapter 5: Failure analysis, including scanning electron microscope and polarized light microscope. Talking about microstructure of solder joint, IMC layer and bulk IMC, crack propagation and failure modes for BGA as well as 2512 Surface Mount Resistor package.
- Chapter 6: Results and conclusions.

Chapter 2

Literature Review

2.1 Introduction

From the previous chapter, it is known that SMT assembly has lots of advantages including higher component density, better mechanical performance, higher real-estate rate, and certainly lower cost. However these advantages make it critical to consider the reliability of electronic packaging. Reliability is defined as the ability of a system or component to function under stated conditions for a specified period of time [48]. Reliability is represented mathematically as the probability of success, or $1 - \text{probability of failure}$ (frequency of failures). Products with bad reliability or failures can increase the costs of both manufacturer and customer. For a manufacturer, failures can increase time-to-market, warranty costs, claims for damages and can damage the reputation of a company and deter new customers. For customers, bad reliability can cause personal injury, increase repair costs, and loss of product capacity, which can impact company market share. Table 2.1 shows the cost of failure in U.S. dollars for different types of business [49].

Table 2.1 Cost of failure for different types of business [49]

<u>Type of Business</u>	<u>Lost Revenue per Hour</u>
Retail Brokerages	\$6,450,000
Credit Card Sales Authorization	\$2,600,000
Home Shopping Channels	\$113,750
Catalog Sales Centers	\$90,000
Airline Reservation Centers	\$89,500
Cellular Service Activations	\$41,000
Package Shipping Services	\$28,250
Online Network Connect Fees	\$22,250
ATM Service Fees	\$14,500
Supermarkets	\$10,000

For reliability in SMT assembly, people consider wafer level reliability, chip level reliability, and board level reliability (BLR), corresponding to the hierarchy of interconnection levels mentioned in Section 1.1, respectively [50]. In particular, Azira, et al. [51] mentioned that board level reliability also known as an interconnect reliability, uses testing to evaluate the quality and reliability of solder connections (BGA, QFN, SMT Resistor, and others) after mounting an IC package to a printed circuit board (PCB). Generally, Matin, et al. [52] mentioned that during a product life cycle, a solder joint would be exposed to an environment of thermal-mechanical fatigue, including temperature excursions, vibration, drop and shock, which can cause the failure of solder joint. A harsh environment will have a severe influence on the board level reliability. Shen, et al. [53] found that fatigue can cause microstructure evolution and deformation due to CTE between SMT components and the printed circuit board. Zhang, et al. [54] investigated solder joint crack propagation along the intermetallic layer of the solder joint between the component and PCB. Zhou, et al. [55] studied the effect of long-term isothermal aging at elevated temperatures on package characteristic lifetime reliability. He cited challenges involving accelerated thermal mechanical test of solder joints, including the difficulty to obtain accurate mechanical properties of bulk solder, large deviations in experimental designs, die sizes, package sizes, ball counts, pitches, mold compounds, and substrate materials, and finally requirement for labor/equipment intensive experiment over years. Basit, et al. [56] developed finite element analysis (FEA) models to simulate solder alloy behavior during thermal aging and cycling. Table 2.2 summaries factors that affect BGA solder joint reliability.

Table 2.2 Factors that affect BGA solder joint reliability

Feature	Lower Reliability	Moderate Reliability	Higher Reliability
Part Type	CBGA	CCGA	PBGA
Die size to part ratio	Largest		Smallest
Ball to pad ratio	Smaller		Larger
Pad type	SMD		NSMD
Via type	In-pad unfilled	In-pad filled	Interstitial open
Via size, min. (aspect ratio)	< 0.020" (> 4:1)		$\geq 0.020"$ ($\leq 4:1$)
Ball size	Smaller		Larger
Stencil thickness	< 0.006"		$\geq 0.006"$
Underfill	Reworkable UF	No UF	Non-reworkable UF

2.2 Effect of IMC on the Reliability

During soldering process in SMT assembly, IMC layers will be generated between the solder paste and the copper pad on the surface of PCB to form metallurgical bond. After soldering, the IMC will continue to grow for the lifetime of the solder joint. Aaron [57] mentioned that the IMC is formed in the reflow oven during the reflow stage, when the solder alloy begins to liquefy or melt. At this time tin in the solder paste will migrate to copper through a process called wetting. The growth of the IMC continues as long as the temperature is above the melting point of the solder alloy. If there is no intermetallic then there is no solder joint. Eric [58] pointed out that the IMC layer is the most brittle part of the solder joint and cracks are easy to propagate along the interface, so that too thick of an IMC layer is bad for joint reliability. Different compositions of an IMC would be formed based on the types of solder pastes applied and surface finishes coated on the copper pad of PCB.

2.2.1 Ag₃Sn IMC

Ma, et al. [59] discovered in tin-rich solder joint, Ag₃Sn IMC is formed due to the reaction between Sn and Ag, as shown in Figure 2.1.

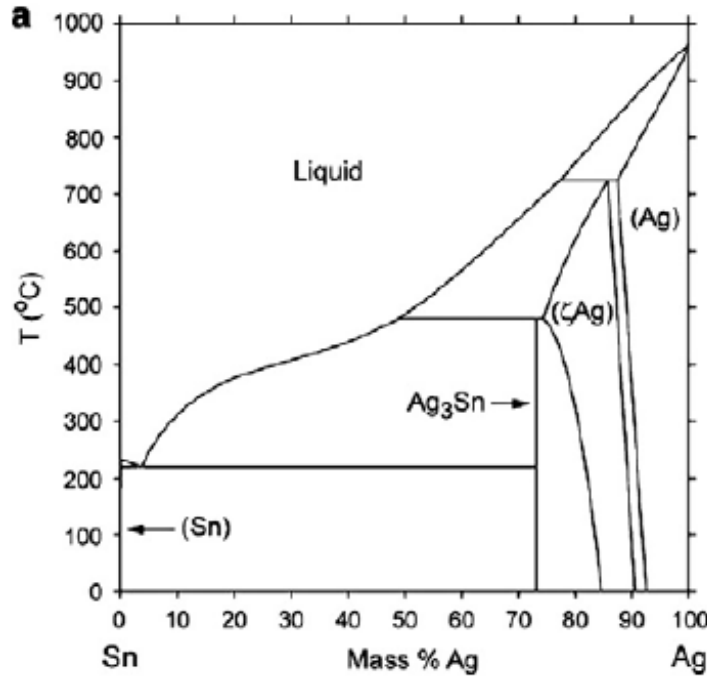


Figure 2.1 Binary phase diagram for Sn-Ag [59]

Wan, et al. [60] concluded that in tin-rich solder joint, the morphology of Ag₃Sn IMC formation was influenced by the cooling rate during the reflow solidification process. Normally there are three types of Ag₃Sn IMC: particle-like, needle-like, and plate-like. Cooling rate determined the size and morphology of Ag₃Sn compound. The sequential evolution of Ag₃Sn IMC morphology with decreasing cooling rate can be summarized as follows: particle-like → needle-like → plate-like. Figure 2.2 shows three types of Ag₃Sn morphology.

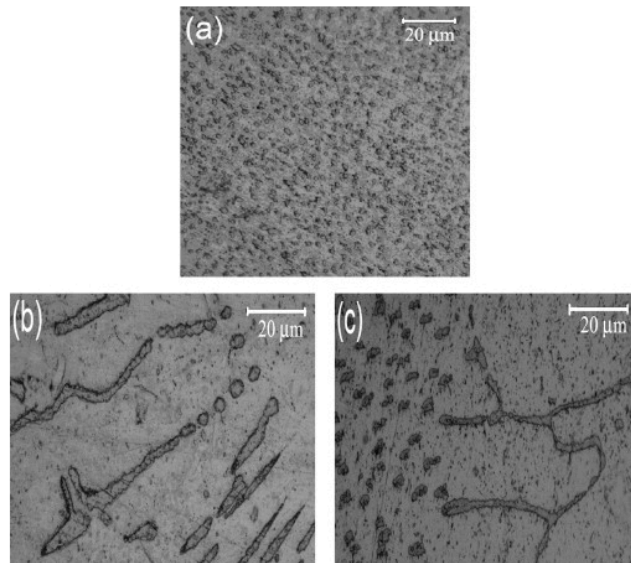


Figure 2.2 Ag_3Sn Morphology: particle-like (a), needle-like (b), and plate-like (c) [60]

Shnawah, et al. [61] mentioned that volume fraction of the fine Ag_3Sn IMC particles in the bulk alloy microstructure of SAC solder alloy increases with increasing Ag, hence, high Ag content SAC solder (SAC305/SAC405) yields large numbers of Ag_3Sn IMC particles and small size of primary Sn grains. On the other hand, low Ag content SAC alloy (SAC105) contains more primary Sn phase (large Sn grains) and fewer of Ag_3Sn IMC particles, as shown in Figure 2.3.

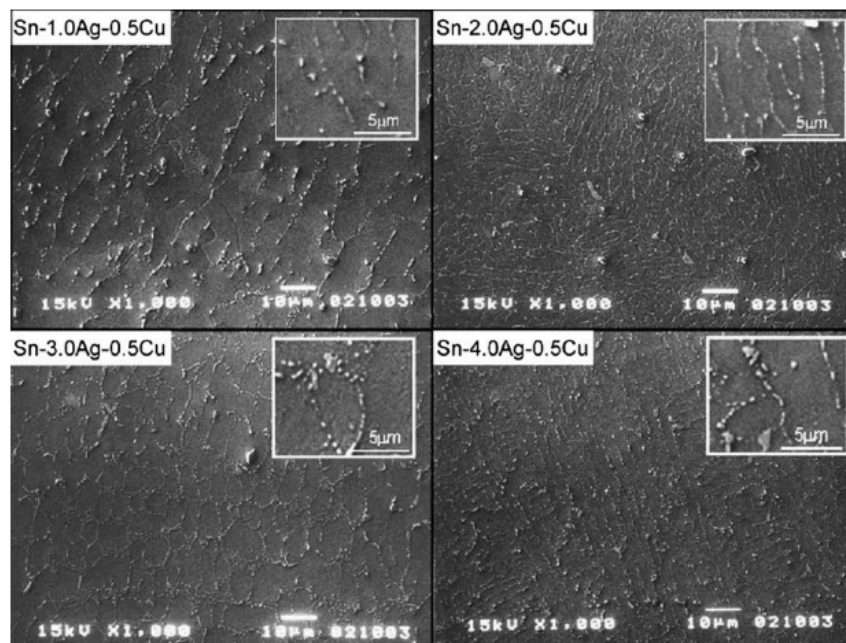


Figure 2.3 The initial microstructure of Sn-xAg-Cu bulk solders [61]

He concluded that the significant thermal cycling performance improvement of SAC305/SAC405 over SAC105 is due partially to the large number of Ag_3Sn IMC particles disperse in the bulk solders, since they can improve the mechanical properties of the solder and suppress the recrystallization during thermal fatigue process. The drop impact performance improvement of SAC105 over SAC305, is due to the low Ag content alloy which has more primary Sn phase in the bulk solder which tends to have low elastic modulus and low yield strength. Kittidacha, et al. [62], Coyle [63], and Lee [64] observed that the presence of a large Ag_3Sn plate can enhance thermal fatigue life by blocking the crack propagation that is initiated at outside corner of the solder joint and grows toward the inside of chip. All of the authors found that more Ag content has a strong positive influence on improvement of thermal fatigue performance, which is in an agreement of Shnawah's study.

2.2.2 Cu-Sn IMC

During reflow and subsequent thermal aging and cycling, Cu-Sn IMC will be formed due to reaction between the Cu substrate and the Sn in the solder paste. Unlike Ag_3Sn IMC which exists mostly in the solder bulk area, CuSn IMC can usually be found at the Component/Solder Joint/PCB interfacial area, and sometimes in the solder bulk [65]. Deng, et al. [66] introduced the IMC layer formation and growth in lead-free solder joints. He found that cooling rate, aging temperature, and aging time played an important role on microstructure evolution and growth kinetics of Cu_6Sn_5 (η -phase) and Cu_3Sn (ϵ -phase). And the CuSn IMC formed between the solder and the substrate greatly influences the thermo-mechanical behavior of the solder joint. Initially, Cu_6Sn_5 growth takes place during reflow when the liquid solder reacts with the Cu substrate, due to substrate dissolution, interfacial reaction and interdiffusion of Sn and Cu. The IMC layer thickness grows with increasing reflow temperature and time. Reflow time and

cooling rate play a role on morphology of CuSn IMC, especially η -phase Cu_6Sn_5 . Shorter reflow time and faster cooling rate lead to a planar morphology, while longer reflow time and slower cooling rate lead to a nodular or scalloped shape as shown in Figure 2.4.

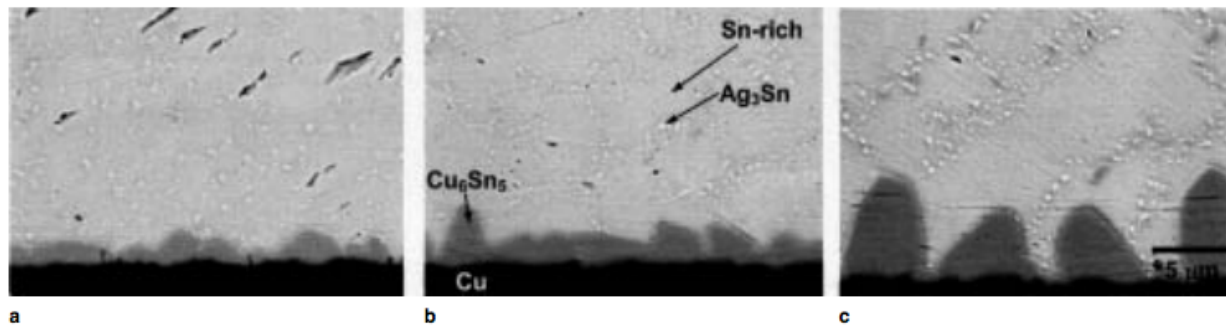


Figure 2.4 Initial morphology of the η -phase Cu_6Sn_5 upon cooling: (a) water quenching, (b) air cooling, and (c) furnace cooling [66]

The author conducted thermal aging test of the SAC 305 joints after reflow, with three temperatures 100°C, 140°C, and 175°C, for aging times varying between 0 h to 1008 h. The evolution of IMC morphology aging at 140°C is shown in Figure 2.5.

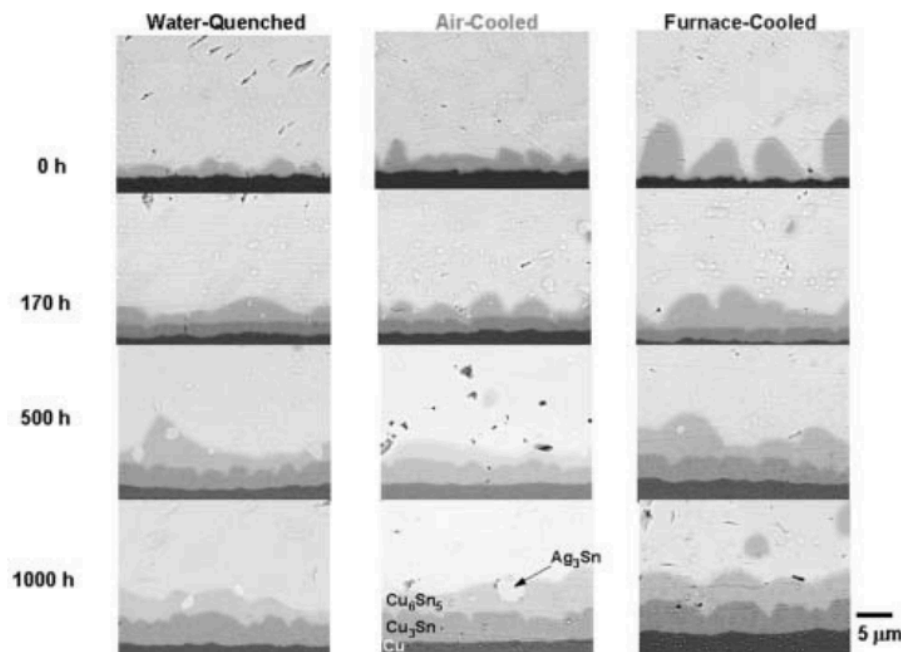


Figure 2.5 Intermetallic morphology development during aging at 140°C [66]

Figure 2.5 shows that during aging, ϵ -phase Cu_3Sn will be formed at the copper pad/ η -phase Cu_6Sn_5 , which appeared to grow with increasing aging time from the reaction of Cu with Cu_6Sn_5 . Zhang et al. [67] also showed the reaction existed in the Cu_6Sn_5 and is represented by the equation; $\text{Cu}_6\text{Sn}_5 + \text{Cu} \rightarrow \text{Cu}_3\text{Sn}$.

Roubaud, et al. [68] did a thermal aging test on lead-free solder joint at 150°C for 32 days. He also observed a similar phenomenon as can be seen from micrograph of CuSn IMC shown in Figure 2.6.

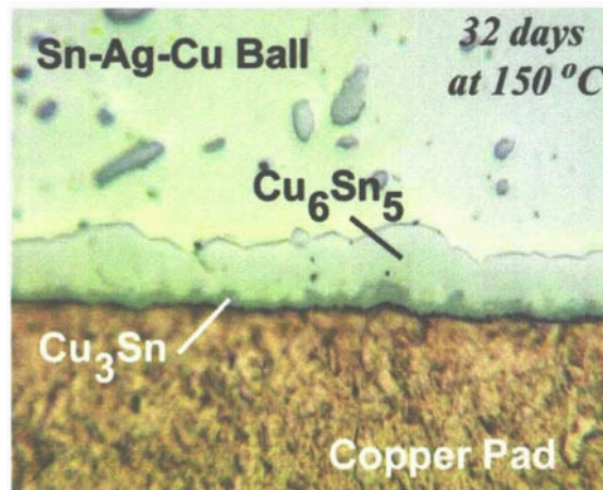


Figure 2.6 IMC at the interface of copper pad and SAC405 after 32 days of aging at 150°C [68]

He also derived a model using parabolic growth kinetics to simulate the thickness growth of these IMC layers:

$$w = w_0 + D\sqrt{t}$$

where: w = thickness of the intermetallic layer

w_0 = initial thickness of the layer

D = Diffusion coefficient

t = time

A similar conclusion has also been obtained by Wassink, et al. [69].

2.2.3 Ni-Sn IMC

If the PCB substrate has a nickel (Ni) coated pad (e.g. ENIG or ENEPIG surface finish), then NiSn IMC will be observed. Che. et al. [70] has conducted research on the PBGA SAC387 solder joint over OSP and ENIG surface finishes. They observed morphology and microstructure changes in the interfacial IMC layer under isothermal aging. They found that after reflow, the IMC were irregular and grow in a needle-like manner and the composition of the IMC is $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ ternary compound. And during thermal aging, small number and tiny $(\text{Ni}, \text{Cu})_3\text{Sn}_4$ IMC started forming between the $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ IMC and the copper pad with Ni coated on top. After further aging the morphology of IMC layer changed from scallop to planar-like and finally layer-like, and became smoother and smoother. Figure 2.7 shows the microstructure change of the IMC layer at the solder/Ni interface under different aging times.

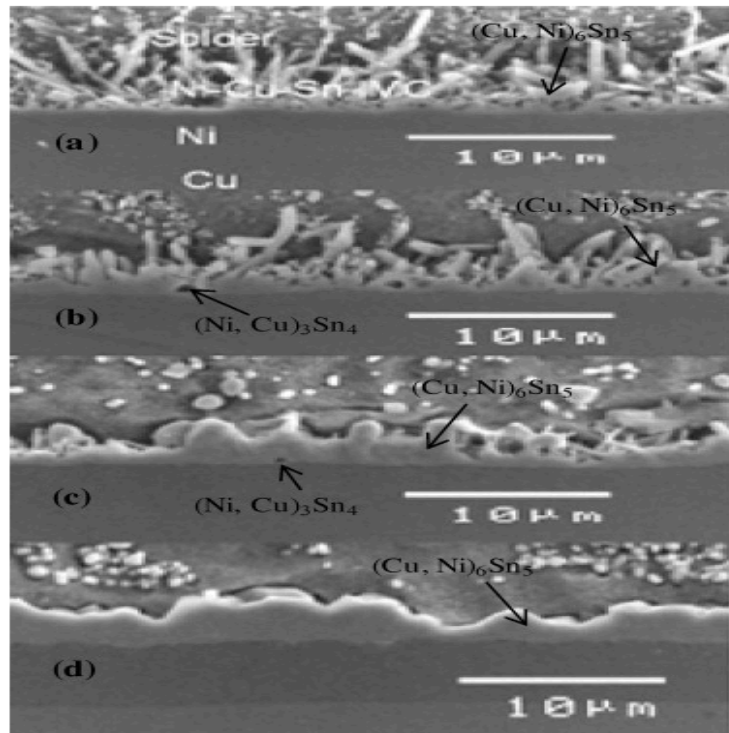


Figure 2.7 Microstructure change of the IMC layer at solder/Ni interface under different aging times, (a) 0 h, (b) 120 h, (c) 260 h and (d) 500 h [70]

Similarly, Alena, et al. [71] showed that the thickness growth rate of CuNiSn IMC is slower because Ni has a much lower diffusivity with Sn than Cu. Figure 2.8 shows a comparison of IMC growth for solder with a HASL surface finish and solder with an ENIG surface finish after 1000 hours of aging. From the figure, one can observe that the thickness for NiSn IMC is much thinner than CuSn IMC. Therefore, Ni is commonly used as a barrier layer to prevent consumption of Cu on the bond pad of the substrate.

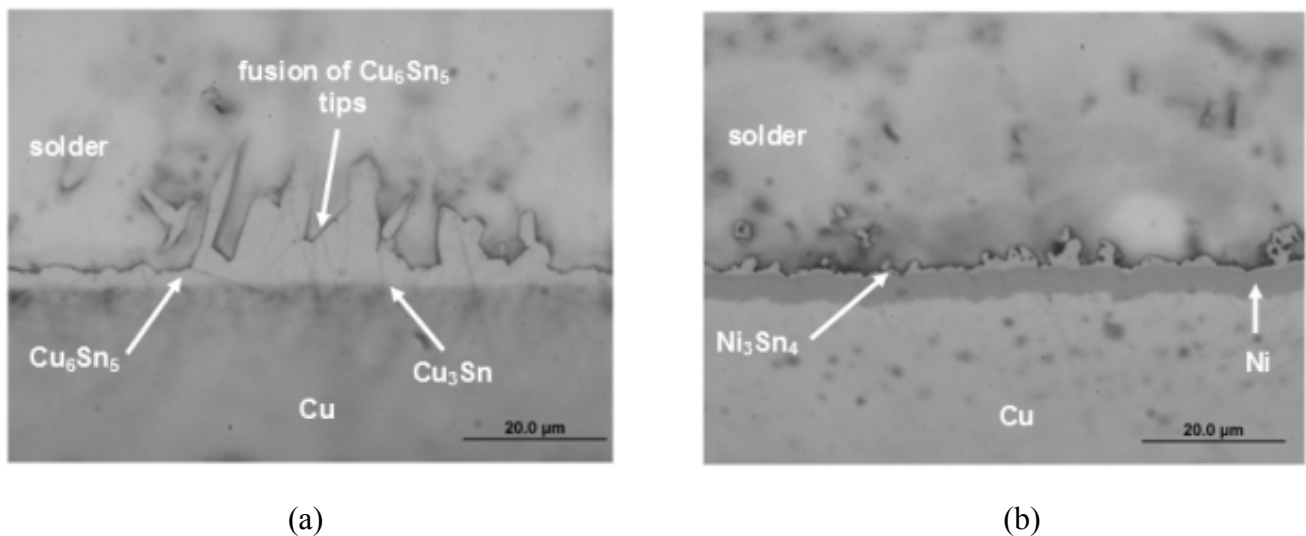


Figure 2.8 Interface of solder-HASL pad interface (a) and solder-ENIG interface (b) after 1000 hours of aging [71]

2.3 Effect of CTE

Electronic packages are subjected to thermally-induced stress due to ambient temperature changes, power cycling, and other reasons. The mismatch of CTE between components and the PCB substrate will induce shear and thermal fatigue to the solder joints, will eventually result in package failure. CTE is used to approximate the linear expansion of a material as a function of the change in ambient temperature:

$$\frac{\Delta L}{L} = \alpha_L \Delta T$$

where: α_L is the coefficient of thermal expansion, ΔT is the change in temperature, L is the original length of the subject, and ΔL is the change in length.

Suhling, et al. [3] presents an analytical model named Distance-to-Neutral Point (DNP) to explain solder joint failure. DNP is a two-dimensional model with a component surface mounted on a PCB. At temperature T_0 , the solder joints induce no stress, and temperature changes to higher and lower are considered. Because the component has much lower CTE than the PCB, the PCB will expand (when temperature increases) or contract (when temperature decreases) much more dramatically than the component, which creates shear strain in the solder joint and leads to thermal fatigue. Figure 2.9 shows an illustration of the DNP Model.

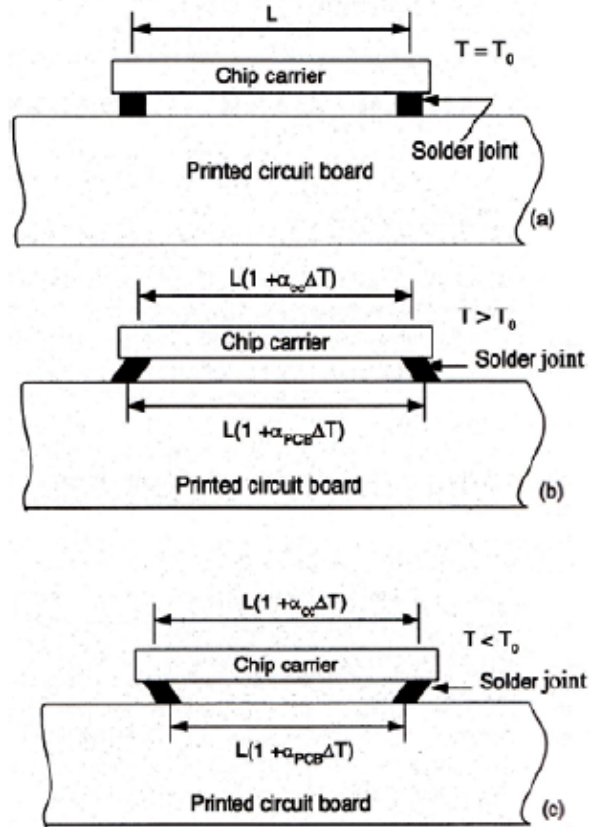


Figure 2.9 DNP model [3]

The shear strain γ is calculated by the DNP model as follows:

$$\gamma = (\alpha_{PCB} - \alpha_{CC}) * \Delta T * DNP / h$$

, where DNP is the distance between the inner edge of the solder joint to the mid-line of the system, ΔT is change in temperature, α_{PCB} and α_{CC} are the CTEs of the printed circuit board and chip carrier, respectively, and h is the height of the solder joint. From the formula we can conclude that induced shear strain increases linearly with DNP, temperature change, and CTE mismatch, as well as decreases with the height of the solder joint. So reliability of the package can be improved by using larger solder joints, controlling CTE mismatch between component and PCB substrate, and limiting temperature fluctuation. Table 2.3 summaries CTE for typical materials used in Electronic Packaging.

Table 2.3 Typical CTE

Material	CTE (x-y axis)ppm/°C	CTE (z axis) ppm/°C
Tin-lead solder	24	24
Copper	16-18	16-18
FR-4	16-18	60-85
Polyimide	15-18	65
BT	15	50
Epoxy Overmold	15	15
Silicon	~2.6	~2.6
Components	6-20	
Alumina oxide	3-6	3-6

2.4 Grain Recrystallization

During thermal aging and thermal cycling, the solder bulk itself will undergo microstructure changes including grain recrystallization, when large grains in the solder bulk will break down into smaller grains and thus generate more grain boundaries. Xu, et al. [71] performed a thermal aging and cycling test on SAC387 with ENIG and OSP surface finish. He observed dynamic recrystallization of Sn-rich phase during thermal cycling aging. Figure 2.10 shows microstructures of the Sn-rich near IMC interface after isothermal aging and thermal cycling.

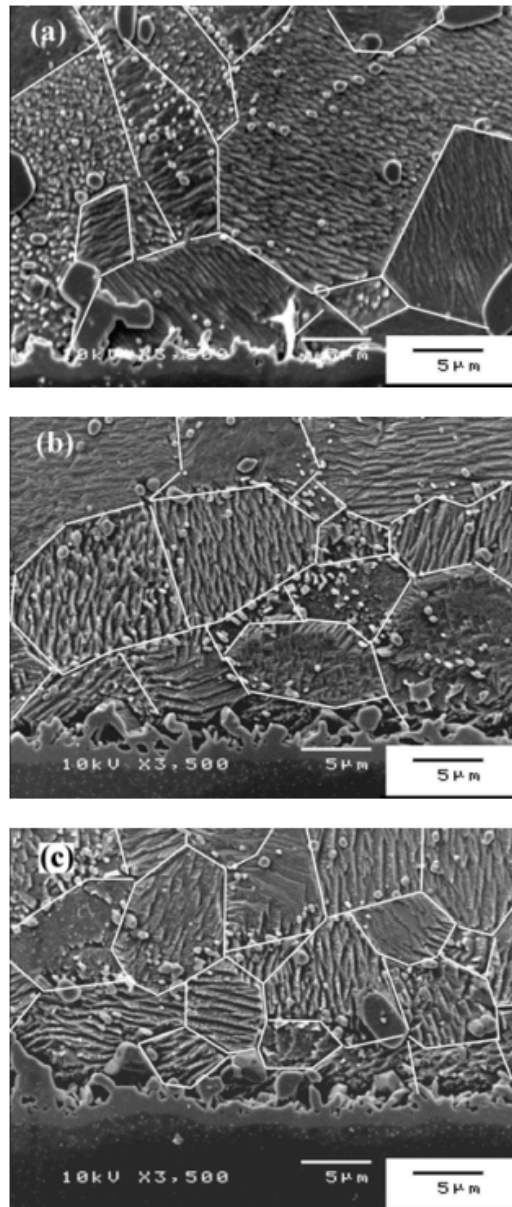


Figure 2.10 Dynamic recrystallization of Sn-rich during thermal cycling (a) as reflowed, (b) 500 thermal cycles, (c) 1500 thermal cycles [71]

The author calculated the average grain size after 500 thermal cycles to be about 13 μm , and after 1500 thermal cycles, the grain size decreases further to only 5-8 μm , while the initial grain size before test was about 20 μm . Decrease of grain size leads to more grains and grain boundaries. The significant change of grain size during thermal cycling indicates that dynamic recrystallization occurred. It is well known that when an alloy is subject to hot deformation, the

processes of strain-hardening and softening are concurrent. Hot deformation may involve the process of dislocation redistribution due to vacancy climb, the formation of recrystallization nuclei and their growth by migration of large angle boundaries under appropriate condition. During the thermal cycling for solder alloy, thermal stress was induced by CTE mismatch in every temperature cycle and caused solder deformation. During the temperature ramp up from -40 to 125°C the dynamic recrystallization occurred, new grains formed and the stress was released. Then, the next temperature cycle came and new deformation was involved before the enlargement of the grains. Berthou, et al. [72] observed the evolution of microstructures on BGA SAC solder balls after 1000 thermal cycles. Figure 2.11 shows an observation with cross polarized light that permits one to see the recrystallization of the Sn macro-grain into small Sn grains. Different colors correspond to the grains with different orientations.

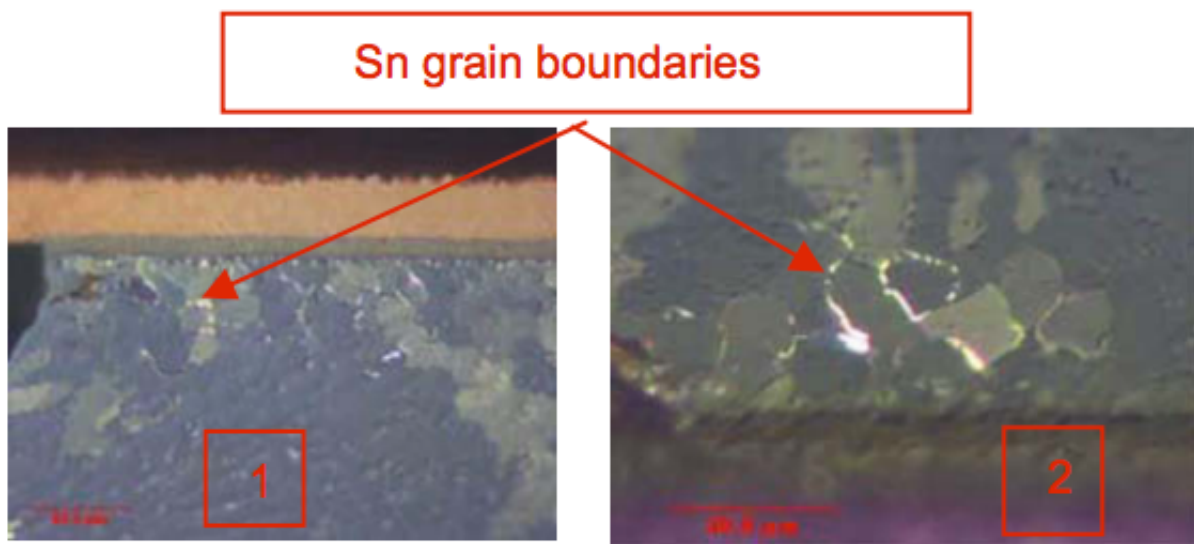


Figure 2.11 Sn Grain Boundaries Under Cross Polarized Light [72]

The evolution of SAC solder joints in thermo-mechanical fatigue is shown in Figure 2.11.

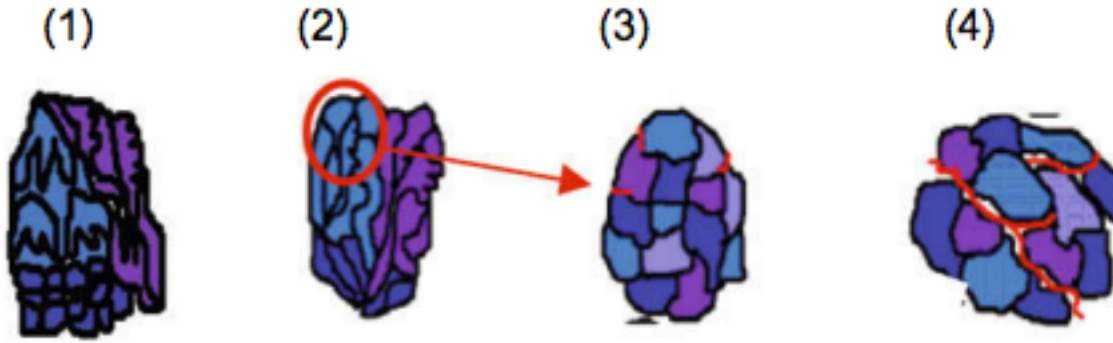


Figure 2.12 Recrystallization phenomenon [72]

From Figure 2.12 [72], the creep relaxation is accompanied by a recrystallization phenomenon. In step (1), the dendritic structure is fine and regular, and with polarized light microscopy it is possible to see the number of dendrite (β -Sn phase) groups having the same crystallographic orientation. At this step the solder joint contains relatively few crystallographically independent dendrite groups. One group represents one Sn macro-grain. In step (2), the number of tin macro-grains is higher than in the first step, and the dendritic structure is rougher. For step (3), the crack initiates along these Sn grain boundaries. And finally for step (4), the crack propagates through the recrystallized zone along tin grain boundaries until electrical opening in solder joint.

2.5 Statistical Weibull Analysis Of Reliability

In electronic packaging, usually Weibull statistics analysis is used to evaluate experimental data from accelerated life testing. A Weibull distribution is used to “fit” the discrete failure data point (in terms of cycles) collected from life testing with continuous functions [73]. The probability density function for Weibull distribution is:

$$f(x) = \left(\frac{\beta}{\theta}\right) \left(\frac{x}{\theta}\right)^{\beta-1} e^{-\left(\frac{x}{\theta}\right)^{\beta}}$$

where beta (β) is referred as the shape parameter, and θ is the characteristic life (in terms of cycles) at which value 63.2% of the population are expected to fail. A Weibull distribution with β and θ parameter is called a two-parameter Weibull distribution. The collected test data are all plotted on a dedicated Weibull probability paper, then a best-fit straight line is drawn to fit the plotted data using a least-squares fitting algorithm. This process is called a goodness-of-fit test. After all these processes are done, the β and θ parameter can be easily obtained from the probability paper to interpret the test result. Computer software, like Weibull ++, Weibull Smith, etc. is now used instead of going through this process by hand. Cong, et al. [74] presented in his paper the Weibull plot for 19mm SAC305 BGA solder joint on ImAg surface finish aging at 125°C up to 24 months which is shown in Figure 2.13.

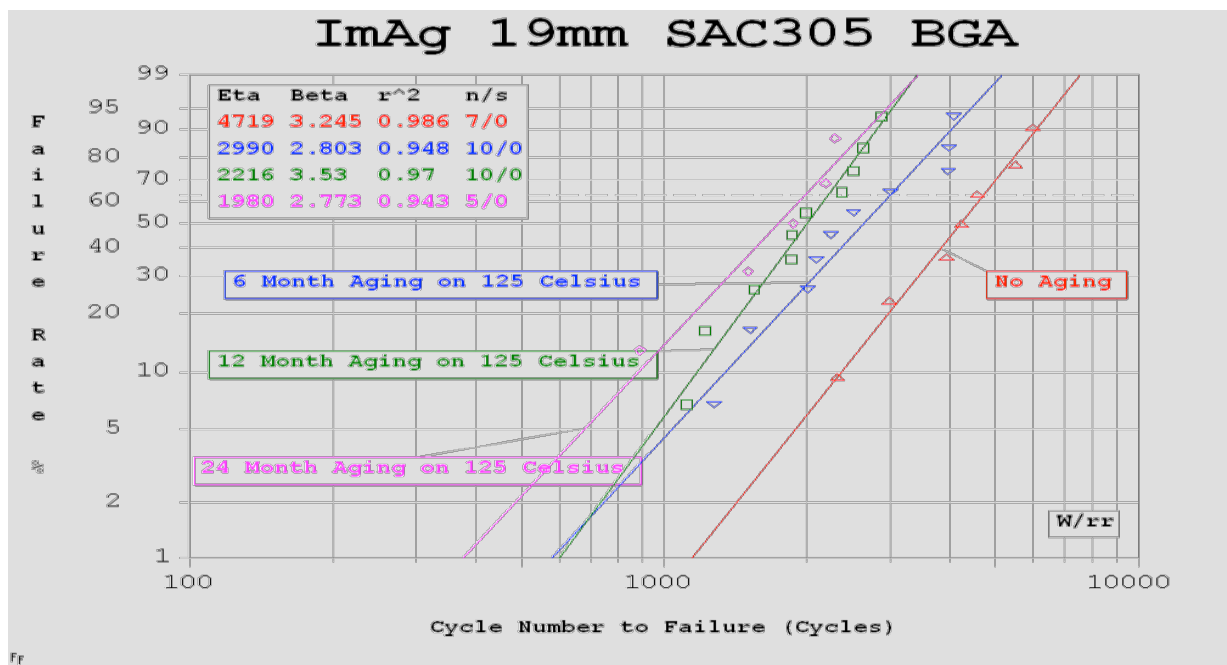


Figure 2.13 Weibull plot for 19mm BGA SAC305 on ImAg aging at 125°C up to 24 months [74]

This 2-parameter Weibull plot is generated by Weibull Smith software. From the Weibull plot, we can get information on the characteristic life parameter θ and the shape or slope parameter β . The higher the characteristic life, the more reliable the solder. For example, the author concluded

characteristic life for 19mm BGA SAC305 on ImAg aging at 125°C and 24 months is 1980 thermal cycles, and for 12 months, 6 months, and no aging group the characteristic life will be 2216, 2990, 4719 cycles, respectively. The author then reached the conclusion that reliability of BGA components subjected to isothermal aging suffers dramatic degradation with longer aging time. On the other hand, the author summarized that the slopes (β) of the Weibull Distributions for SAC105 solder are in the range of 5.0-8.0, and the slopes for SAC305 solder are around 3.0. In general, lower slope values indicate slower failure rates or a greater time between failures, and hence greater variance in the failure data. This also means that it is more difficult to predict when failures will occur. Along with lower slope values, the SAC305 configurations also had higher characteristic lifetimes than those for SAC105. Lower slopes could have also increased the probability for early failures.

2.6 Failure Modes

Solder joint failure mechanisms resulting from the influence of CTE mismatch, IMC growth, microstructural change during isothermal aging and cycling, grain recrystallization, creep, as well as fatigue have been introduced. Typical failure modes of solder joint should also be investigated. Zhou [75] listed in his Ph.D. dissertation that common BGA solder joints had two failure modes: cracks propagated along the near-interfacial IMC layer or cracks through the bulk solder area, as shown in Figure 2.14.

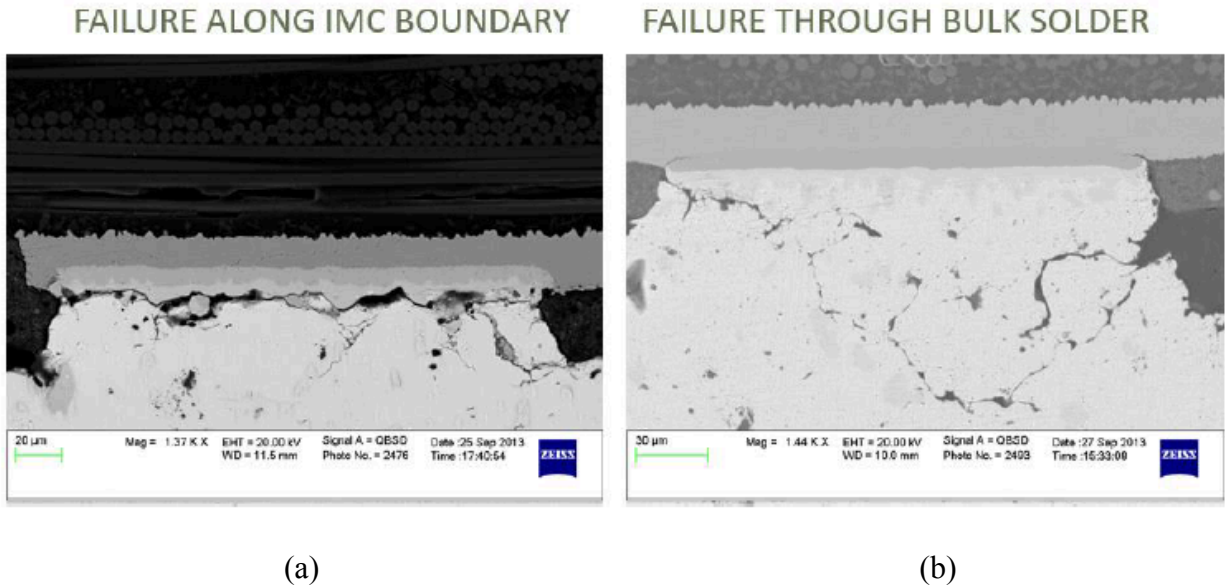


Figure 2.14 Common BGA solder joint failure modes: crack propagates along near-interfacial IMC layer (a), and crack propagates through bulk solder [75]

A crack usually initiates at the highest stress concentration area, which is the upper and lower corner of the solder joint. Cong, et al. [76] proposed a typical solder joint failure mode for a surface mount resistor. He found that the crack initiates at the inside of the joint and propagates underneath the component termination and then outward through the primary fillet until an open circuit occurred, shown in 2.15.

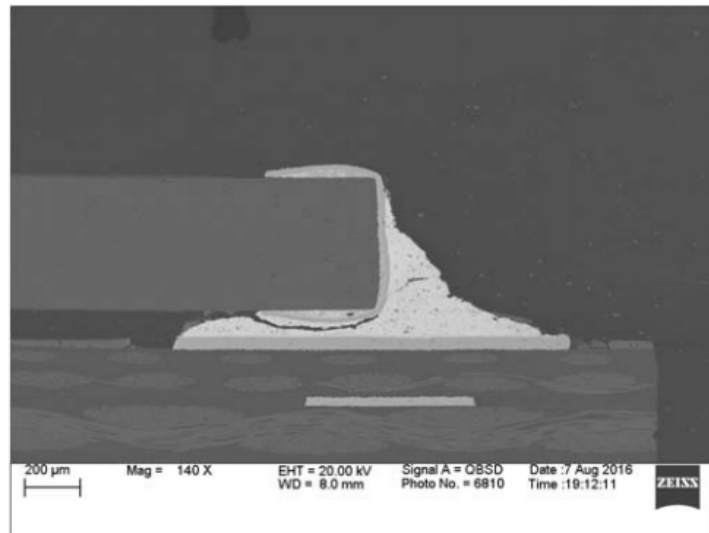


Figure 2.15 Typical failure mode for surface mount resistor [76]

2.7 Accelerated Life Testing

Accelerated life testing (ALT) is the process to test a product subjected to environmental conditions such as strain, stress, temperatures, voltage, vibration, drop, thermal aging, thermal cycling etc., in excess of its normal working parameters in order to discover potential failures in a short period of time. Engineers can make predictions for the reliability performance of the product to help them deal with design for reliability (DFR) or design for manufacturing (DFM), by analyzing the life testing result. So ALT is essential in both product development stage and maintenance after it is purchased by the customer [77]. Nemeth, et al. [78] listed in his book a variety of reliability life tests used when assessing electronic assemblies:

1. Thermal cycling (TC): product is tested by cycling through two temperature extremes above what the actual use requires, typically at high rates of change. TC is an environmental stress test used to catch latent defects by inducing failure through thermal fatigue and creep. TC test is based on JEDEC Standard “JESD22-A104D”. Figure 2.16 shows representative temperature profile for thermal cycle test conditions.

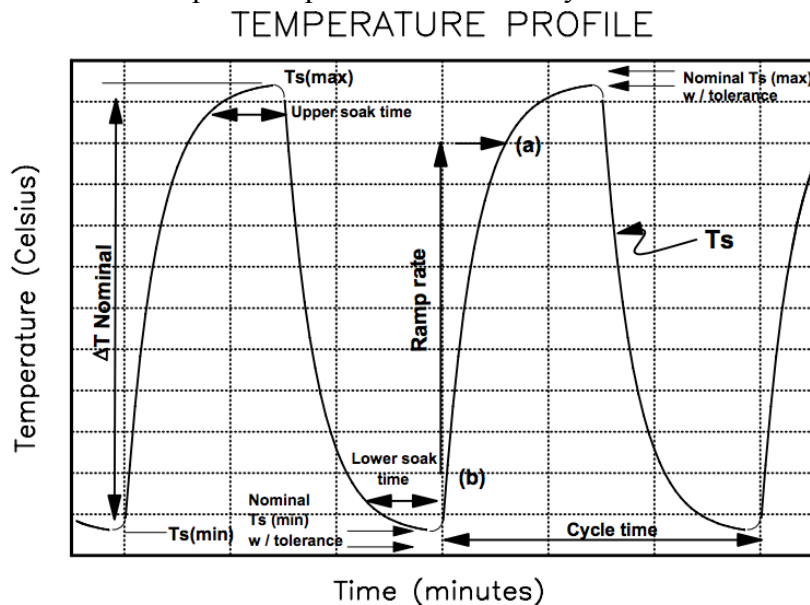


Figure 2.16 Temperature profile for thermal cycle test conditions [78]

During TC testing, the product will cycle through ramp up, upper soak or dwell, ramp down, and lower soak or dwell stages. Important factors of a thermal cycling test are dwell temperatures, dwell times and ramp rates. During each cycle the product or test vehicle experiences thermo-mechanical fatigue that finally leads to failure. Qi, et al. [79] investigated the impact of ramp rate and temperature range on lead-free and tin-lead solders. They found that the higher ramp rate reduced the testing time while retaining the same failure modes, and that the damage per cycle increased with the temperature difference. Raza, et al. [80] gave the acceleration factor (AF) relationship as a function of the Coffin-Manson Exponent, which is a ratio of the product life at normal operating conditions to the life at accelerated test conditions:

$$AF = \left(\frac{f_0}{f_T}\right)^q \left(\frac{\Delta T_T}{\Delta T_O}\right)^c e^{1414\left(\frac{1}{T_0} - \frac{1}{T_1}\right)}$$

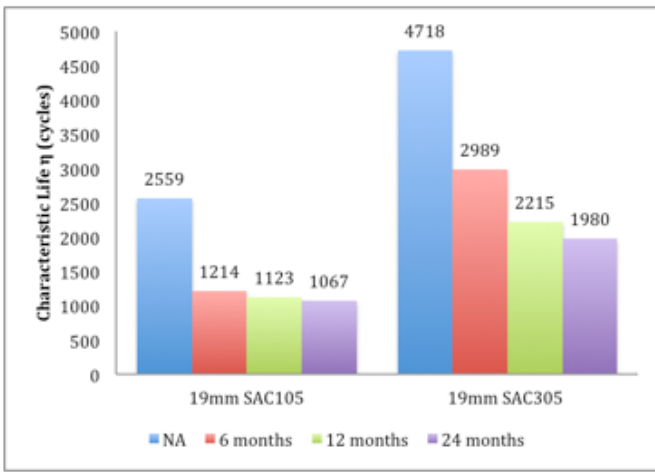
where the subscripts T and O stands for testing and operating conditions, respectively, f is the thermal cycling frequency, and T and ΔT are the temperature and temperature range in degrees Celsius. For SnPb solders, typical values used for the parameters q and c are: q = -0.33 and c=1.9 [81], and for SAC solders, m=0.33, n=1.9 [82].

Thermal shock testing is a special case of thermal cycle testing where the ramp rate is approximate infinite. Thermal cycling and thermal shock tests are conducted in an air or liquid chamber. Table 2.4 lists recommended dwell temperatures for TC testing by application [83].

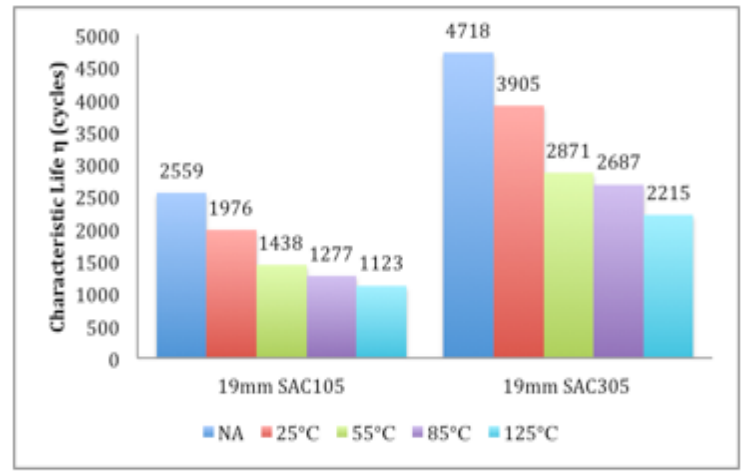
Table 2.4 Dwell temperatures for TC testing by application [83]

Market	Low Temperature	High Temperature
Consumer	0°C	70°C
Telecommunications	0°C	100°C
Industry	-40°C	85°C
Automotive	-40°C	125°C
Military	-55°C	125°C

2. Thermal Aging: a product is tested at a constant elevated temperature for an extended duration. Thermal aging testing is used to simulate the effect of shelf life, which is the length of time that a product is stored without being used by customer, on the reliability of the product. Thermal aging can induce high levels of stress and cause creep failure. Isothermal aging testing is usually performed before a thermal cycling test. Dr. Evans research group at Auburn University has conducted numerous studies that demonstrated severe reliability problems caused by long-term isothermal aging in elevated temperatures [83-86]. As an example, Figure 2.17 shows the characteristic life degradation chart for BGA SAC solder joints with various aging times and temperatures.



(a)



(b)

Figure 2.17 Characteristic life degradation chart for BGA SAC solder joints with various aging times (a) and temperatures (b)

From Figure 2.17 one can conclude that the reliability of BGA components subjected to isothermal aging suffer dramatic degradation with longer aging times and higher aging temperatures. The reliability can degrade up to 70% as a result of two years aging.

3. Drop Test: examines the mechanical integrity of the product under a mechanical shock, by raising the test vehicle to a specific height and then releasing it for a free-fall drop. The JEDEC Standard JESD22-B104C can be used for half-sine waveform. Farris, et al. [87] concluded in his paper that first the component location plays a significant role in the drop test reliability. Generally speaking, components at the center of the board are more prone to fail due to higher stains. Second, higher impact force resulted in lower drops-to-failure. And finally, the majority of drop test failures were trace breaking caused by cohesive failure of the resin between the copper pads and the fiberglass dielectric layer, which indicated that solder joints are not the weakest link area of the assembly. Lee, et al. [88] proved that SAC105 has better drop test reliability than SAC305.

2.8 Solder Doping

With the need for better drop resistance, many lead-free BGAs are being made in alloys other than SAC305. Since SAC305 has significantly lower drop resistance when compared to Sn63/Pb37, component manufacturers have been moving away from this type of alloy and towards alternative lead free alloys such as SAC105 in applications involving significant drop and vibration. There also are many alloys competing for market share that are SAC lead free solder family plus a fourth element, often referred to as a dopant, such as antimony (Sb), magnesium (Mg), nickel (Ni), cobalt (Co), or indium (In). These additives create finer grain boundaries and reduce the intermetallic formations of the tin with silver or copper, resulting in a more reproducible grain as well as a more uniform grain formation in the lead-free alloy. This process is called solder doping, or solder micro-alloy, or solder addition [89]. Currently, a limited number of solders designed for high-temperature reliability are available on the market, and more are in development. These new alloys are targeted for use in harsh environments requiring resistance to both thermo-mechanical (accelerated thermal cycling) and mechanical (vibration, bending, and shock) loading. The alloys are being designed to improve toughness and thickness of interfacial intermetallic layers and provide solid solution strengthening to compensate for the loss of strength once the Ag_3Sn particles coarsen, and limit the amount of copper diffusion.

This dissertation considers reliability for a variety of different electronic components with more than 10 SAC lead-free solder joints with dopants, under the effect of long-term isothermal aging and thermal cycling.

Chapter 3

Experimental Setup

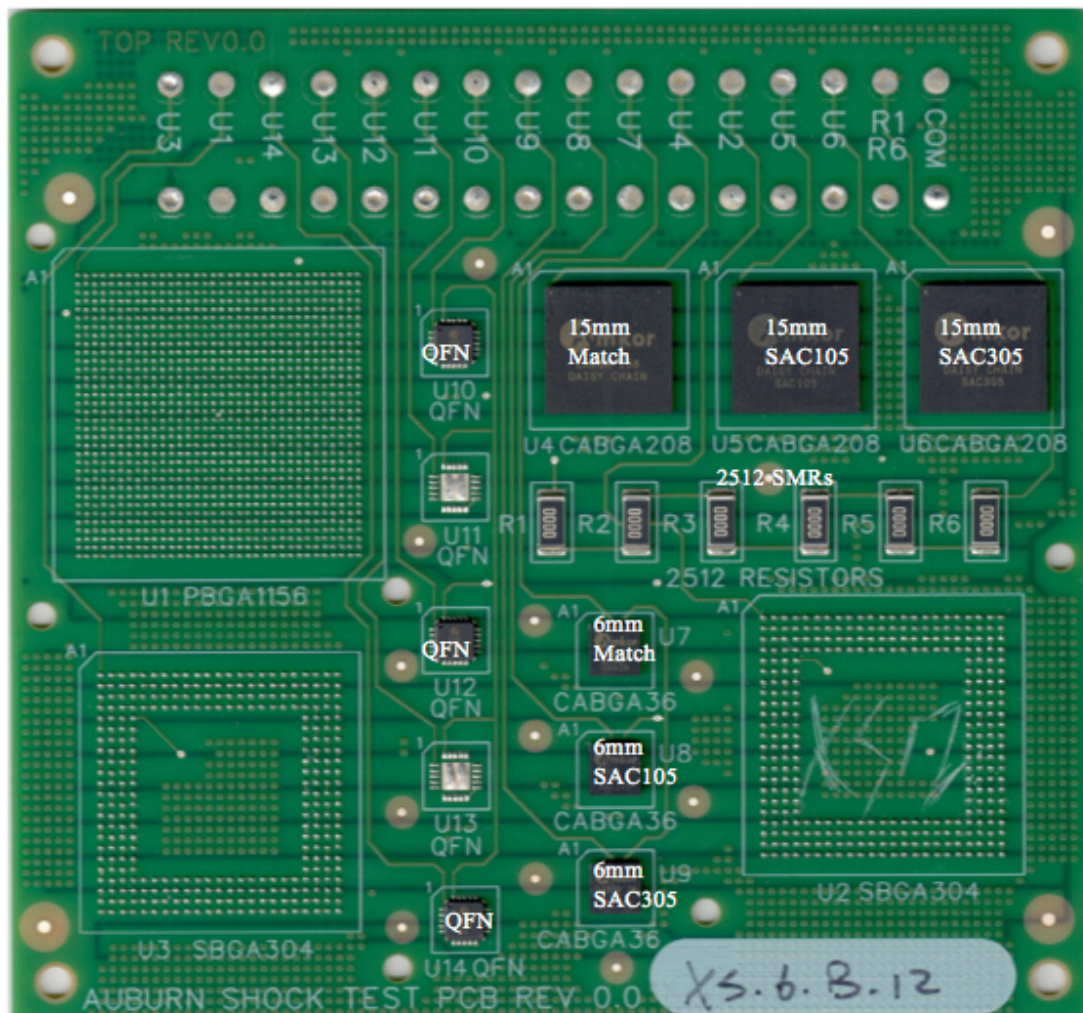
3.1 Introduction

The electronic packaging industry has been undergoing transition toward the use of more compact and more reliable packages to meet market demand. In order to eliminate environment and health hazards the industry has banned tin-lead and moved to lead-free solder. Electronic packages are subjected to thermal-mechanical induced stress when operating. The industry still has limited knowledge on board level reliability for SMT components with solder joints, especially when the package is under a harsh environment such as long-term isothermal aging and cycling in elevated temperature. Also limited research has been done investigating many factors affecting the board level reliability of the solder joints, including package size, package type, pitch size, BGA arrangement, surface finish, solder with dopant, and various thermal aging times and temperatures. The failure mechanisms as well as failure modes for solder joints with dopant have been seldom investigated. So the purpose for this project is primarily to find a manufactureable solder paste with dopants that can mitigate the effects of aging. A secondary goal is to find a solder material for solder-sphere replacement to enhance individual package reliability. In this dissertation, we test a full experimental matrix including various selections of solder alloys, doped solder pastes, package sizes and pitch sizes, surface finishes, isothermal aging time up to 12 months, and isothermal aging temperatures up to 125°C, followed by thermal cycling testing. Failure mechanisms and failure modes for solder paste with dopant have also been summarized.

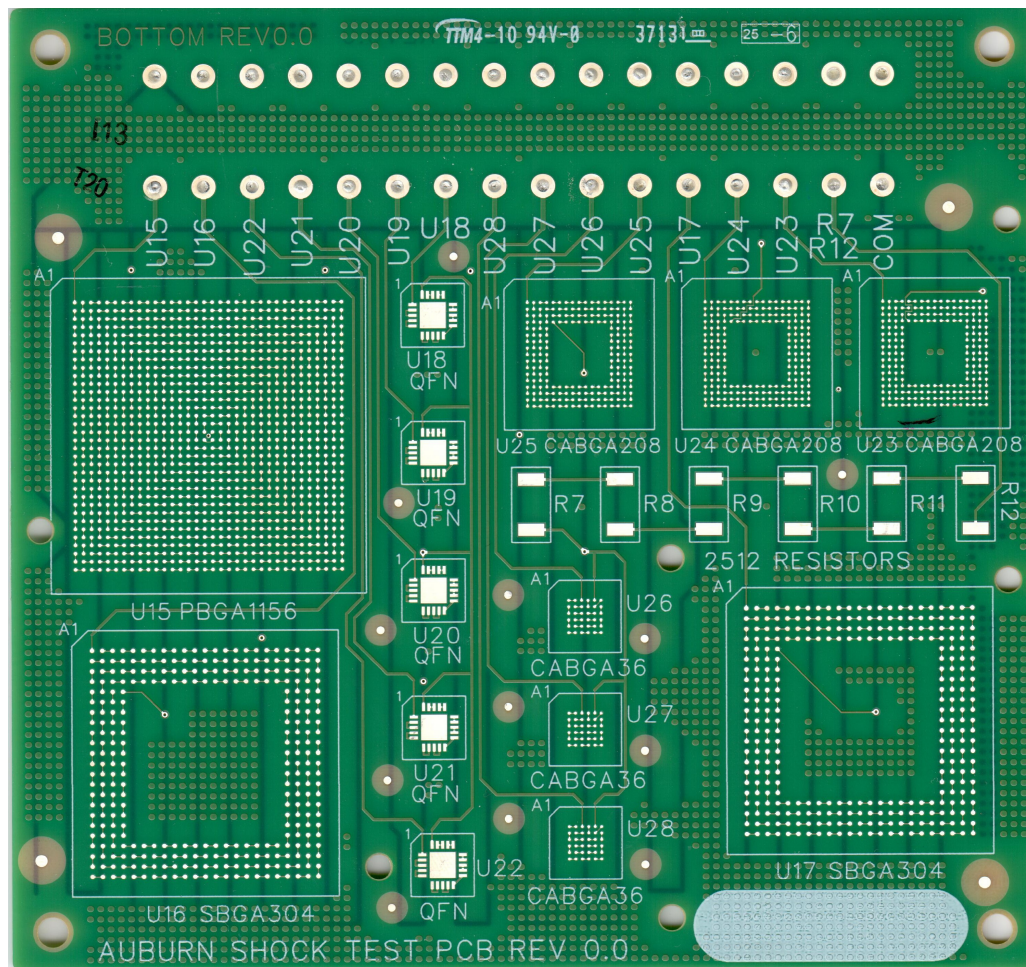
3.2 Test Vehicle (TV) Design and Assembly

3.2.1 Test Board Design (TV9)

The assembled test vehicle consists of a FR4-06 glass-epoxy PCB with a base glass transition temperature of 170°C. The dimensions of the board are 4.0 x 5.0 x 0.062 inches. Non-solder mask defined (NSMD) pads were used. Test vehicles with three different surface finishes are tested: OSP, ImAg, and ENIG. Figure 3.1 shows a schematic of the test vehicle frontside (with components assembled) and backside.



(a)



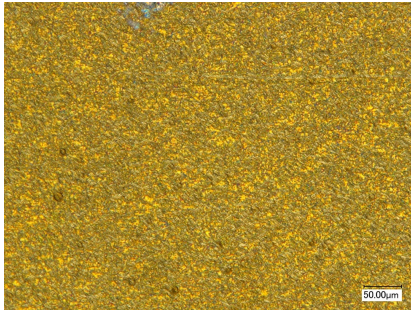
(b)

Figure 3.1 Test board design of frontside (a) and backside (b)

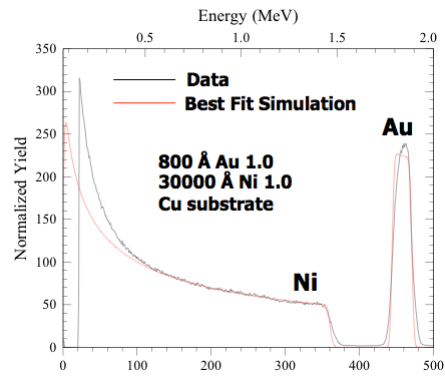
Rutherford backscattering spectroscopy (RBS) is used to measure the metallic layer's thickness of starting surface finishes, to enable later comparisons after long term thermal aging and cycling.

Figure 3.2 shows test results from RBS on each of the three surface finishes

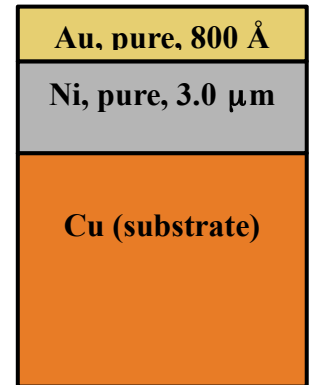
Surface Appearance



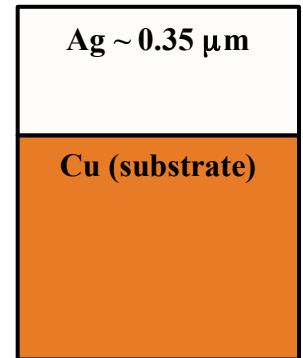
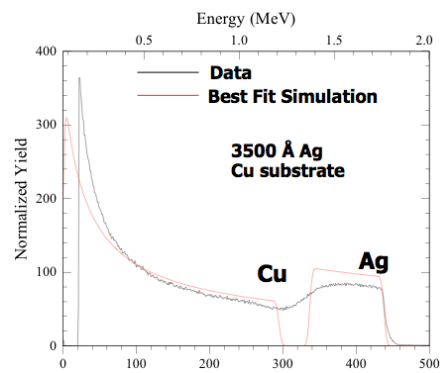
Channel



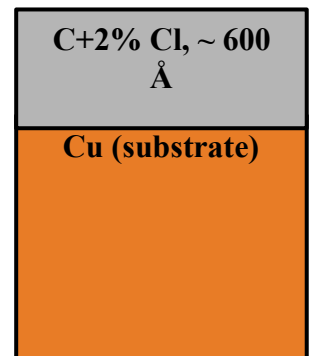
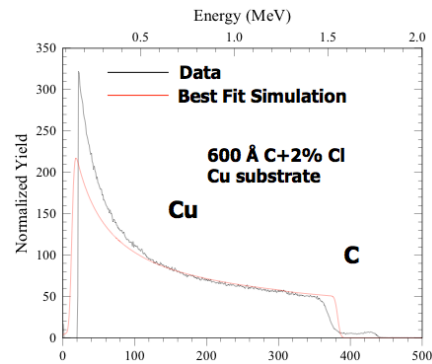
Thickness



(a)



(b)



(c)

Figure 3.2 RBS for surface finishes: (a) ENIG, (b) ImAg, (c) OSP

The RBS spectra shows that the starting board finish layers are relatively sharp, although a slight “rounding” of the leading and trailing edges of the RBS peaks for the Au and Ni layers (compared to simulation) indicates interfacial roughness and/or slight inter-diffusion between the layers. For the ENIG surface finish, we can see the Au layer is on top of Ni layer, and Ni layer is more than 30 times thicker than the Au layer. For ImAg, it is the Ag layer coated on top of copper pad. For the OSP surface finish, the coating layer has the thinnest thickness compared to the other two.

3.2.2 Test Components

TV9 consists of both active and passive components, including BGA package, micro lead frame (MFL) QFN package, and 2512 SMRs. Plastic BGA components are mounted on the PCB using second-level interconnects (solder joints) of paste-doped Sn-1Ag-0.5Cu (SAC105) and Sn-3Ag-0.5Cu (SAC305), as well as matched doped solder joints (paste and spheres of matching composition) with package sizes of 6mm x 6mm, and 15mm x 15mm, and 0.8mm pitch size. The package size for MLF QFN is 5mm x 5mm. 2512 SMRs are selected for comparison due to their large body size, high rated power dissipation, and poor solder joint reliability. They are mounted in banks of six resistors placed in series. QFNs and 2512 SMRs are incorporated on the test vehicle with terminations of 100% Sn. All test components are provided by Practical Components with daisy chain connection so that an electrical signal will pass through each solder joint of the component in series, allowing for continuous sampling of component resistance to detect solder joint failures immediately. These components are “dummy die” components, whose dies are non-functioning during testing. All tested components are presented in Table 3.1.

Table 3.1 Test component matrix

Package Type	Package Size (mm)	Pitch Size (mm)	Die Size (mm)	Ball Diameter (mm)	I/O Count	Ball Arrangement	Solder Joint
BGA	15x15	0.8	12x12	0.46	208	Perimeter	SAC105 SAC305 MATCH
BGA	6x6	0.8	NA	0.46	36	Full Array	SAC105 SAC305 MATCH
QFN	5x5	0.65	4.5x4.5	NA	20	NA	Paste Only
2512 SMR	2.5x1.2	NA	NA	NA	NA	NA	Paste Only

The 15mm BGA has a perimeter ball arrangement, and the 6mm BGA has full array ball arrangement. Figure 3.3 shows bottom view of 15mm BGA and 6mm BGA.

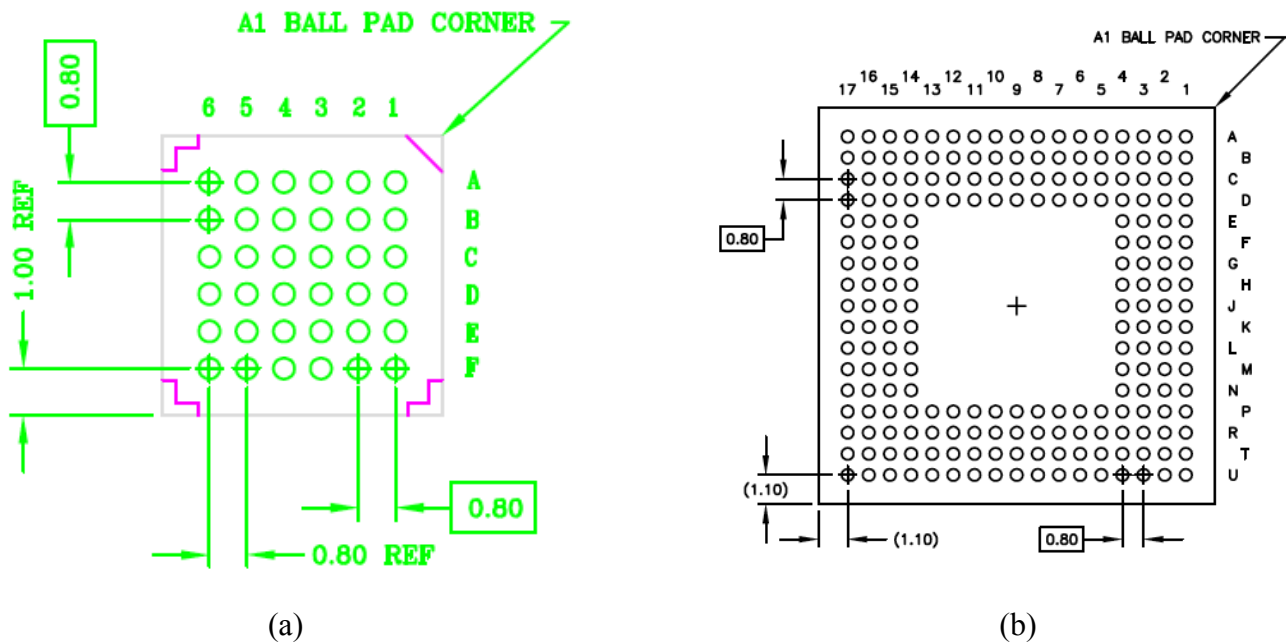


Figure 3.3 Bottom view of BGA package: (a) full array 6mm BGA, (b) perimeter 15mm BGA

3.2.3 Solder Pastes

Fourteen lead-free solder pastes with dopants supplied by 8 companies (Indium, Alpha, Senju, Accurus, Heraues, Henkel, AIM, Inventec) are selected for testing. BGA packages are pre-balled through balling process with SAC105, SAC305, and matched solder sphere (same alloy with doped solder pastes) before placed on PCB copper pad with stencil printed doped solder paste.

Due to materials availability, some BGAs lack the matched solder sphere. Table 3.2 summaries all tested doped solder pastes information.

Table 3.2 Solder paste information

Paste Name	Paste Code	Paste Alloy Composition	BGA Pre-Balling Sphere	
			15mm BGA	6mm BGA
Indium Material 1	Paste A	98.47Sn-0.5Ag-1.0Cu-0.03Mn	SAC105 SAC305 MATCH	SAC105 SAC305 MATCH
Alpha Innolot	Paste B	90.95Sn -3.80Ag-0.70Cu-0.15Ni - 1.40Sb-3.00Bi	SAC105 SAC305 MATCH	SAC105 SAC305 MATCH
Indium Material 2	Paste C	SAC+Sb	SAC105 SAC305	SAC105
Senju M794	Paste D	Sn-3.4Ag-0.7Cu-3.2Bi-3.0Sb-Ni-x	SAC105 SAC305 MATCH	SAC105 SAC305 MATCH
Alpha Maxrel +	Paste E	Sn-3.8Ag-0.8Cu-Bi-X	SAC105 SAC305 MATCH	SAC105 SAC305 MATCH
Accurus CycloMax	Paste F	92.77Sn-3.41Ag-0.52Cu-3.3Bi	SAC105 SAC305 MATCH	SAC105 SAC305 MATCH
Accurus Ecolloy	Paste G	96.62Sn-0.92Cu-2.46Bi	SAC105 SAC305 MATCH	SAC105 SAC305 MATCH
Heraeus Innolot	Paste H	Sn-3.5Ag-0.7Cu- 0.125Ni-1.5Sb-3Bi	SAC105 SAC305	SAC105
Heraeus HT 1.02	Paste I	Sn-2.5Ag-0.5Cu-2In-0.03Nd (Crystal modifier)	SAC105 SAC305 MATCH	SAC105 SAC305 MATCH
Senju M758	Paste J	Sn-3.0Ag-3Bi-0.8Cu-Ni	SAC105 SAC305 MATCH	SAC105 SAC305 MATCH
Henkle K	Paste K	95.5Sn-3.8Ag-0.7Cu-0.02Ni-1.5Sb-3Bi	SAC105 SAC305	SAC105
Henkle L	Paste L	95.5Sn-3.8Ag-0.7Cu-0.02Ni-1.5Sb-3Bi	SAC105 SAC305	SAC105
AIM	Paste M	NA	SAC105SAC305	SAC105 SAC305
Inventec	Paste N	95.35Sn-4Ag-0.5Cu-0.05Ni	SAC105 SAC305	SAC105 SAC305

From Table 3.2 we can conclude that doped solder pastes are created by adding SAC solder paste families with a fourth or more elements. In this research, Bi, Sb, Ni, Mn, Nd, and In are included as the dopants.

3.2.4 TV SMT Assembly

All Test Vehicles TV9 are assembled in the University of Alabama at Huntsville (UAH) Electronics Packaging Lab. A 12-hour 'bake out' process is performed before assembly in the oven at 150°C to remove moisture and potential damage to the assembly during reflow. An E-FAB Electroform stencil is used for stencil printing, the thickness of which is 0.006 inch. The solder paste print machine used was an MPM UP2000 HiE. After solder paste is stencil printed on the PCB substrate, the assembly will be inspected and verified by a 3D inspection process to check the area and the volume of the paste deposit. Then the assembly is transferred to a Universal GSM-1 pick-and-place machine with a tray feeder to pick and place all the components. The machine has pre-stored programmed algorithm to pick and place all test components onto the test vehicle correctly in order. The board was checked again in case of skewed package placement. Figure 3.4 shows a picture for the entire SMT assembly line at UAH.



Figure 3.4 SMT assembly line at UAH

The assembly is reflowed in a 13-zone Rehm V7 convection reflow oven. The oven has a conveyor speed of 26 inch/min and operates within a nitrogen gas environment. The reflow thermal profile has been determined through testing to make sure the solder joints have the best wetting and least board damage. The oven is shown in Figure 3.5, and the reflow profile is shown in Figure 3.6. The preheat time (from 35°C to 155°C) is around 80 seconds, with a soak time (from 155°C to 175°C) duration around 75 seconds. Peak temperature is around 245°C. Total time above 217°C (melting point for SAC alloys) is about 70 seconds. Max temperature rising rate is about 3 degrees per second.



Reflow Oven: Rehm V7

Figure 3.5 Reflow oven

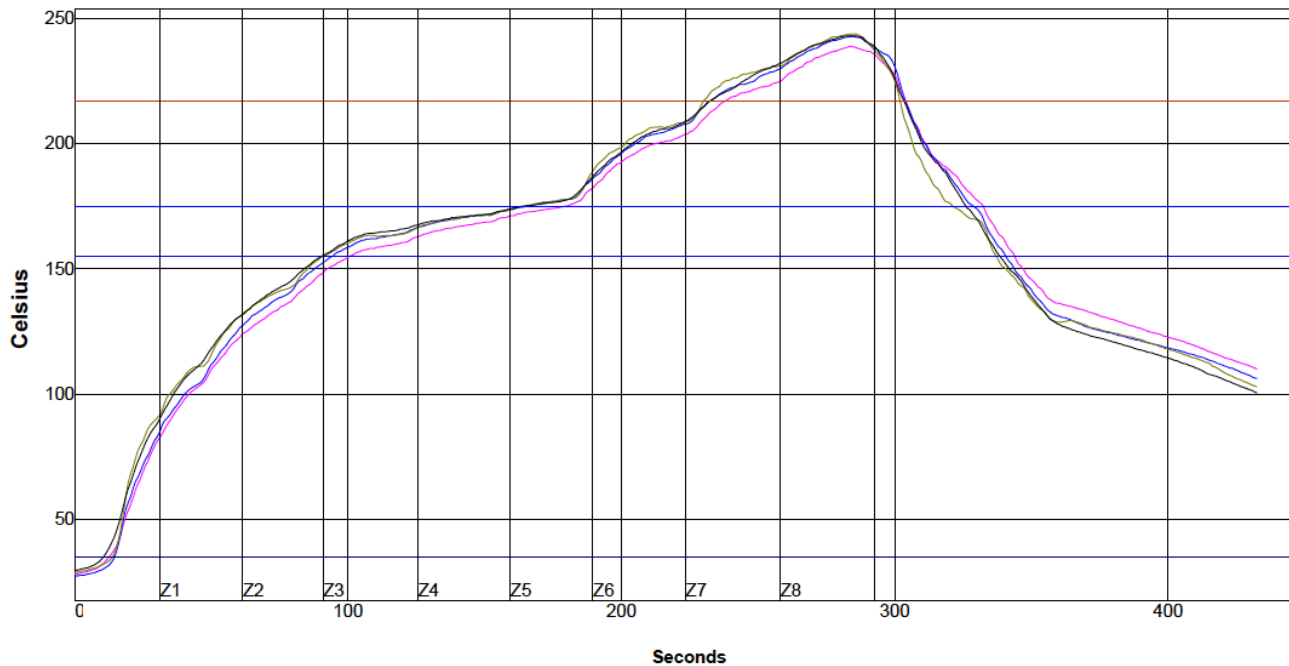


Figure 3.6 Reflow profile

After reflow, a transmission X-ray tomography system was used to inspect the quality of the solder joints in the assemblies. Defects such as insufficient solder, solder bridging, voids in joints, black pad, and head-in-pillow can be detected with this technology. Any manufacturing defect is reworked.

3.3 Thermal Test

3.3.1 Isothermal Aging and Thermal Cycling Test Matrix

Test vehicles with Paste A to L were subjected to isothermal aging at temperature 125°C with 12 months aging time. Paste B, C, and K also have no-aging control specimens for comparison. Paste M and N have only the no-aging group. Subsequent to aging, all test vehicles are put together in the 16 ft³ Thermotron thermal cycling chamber. The thermal cycling test profile was based on a modified standard JEDEC JESD 22-A104-B due to a limitation of the chamber hardware. The thermal cycles ranges from -40°C to 125°C, with 15 minutes dwell time at upper

peak temperature, and 10 minutes at lower peak. Both ramp up and ramp down time are 50 minutes. Table 3.3 summaries isothermal aging test matrix. Figure 3.7 shows thermal cycling test profile.

Table 3.3 Isothermal aging test matrix (tabular number stands for number of test vehicles)

Aging Doped Paste	12 months Aging at 125 °C			No Aging		
	OSP	ImAg	ENIG	OSP	ImAg	ENIG
Paste A	5	5	5			
Paste B	5	5	5	5	5	5
Paste C	5	5	5	5	5	5
Paste D	5	5	5			
Paste E	5	5	5			
Paste F	5	5	5			
Paste G	5	5	5			
Paste H	5	5	5			
Paste I	5	5	5			
Paste J	5	5	5			
Paste K	5	5	5	5	5	5
Paste L	5	5	5			
Paste M	0	0	0	5	5	5
Paste N	0	0	0	5	5	5

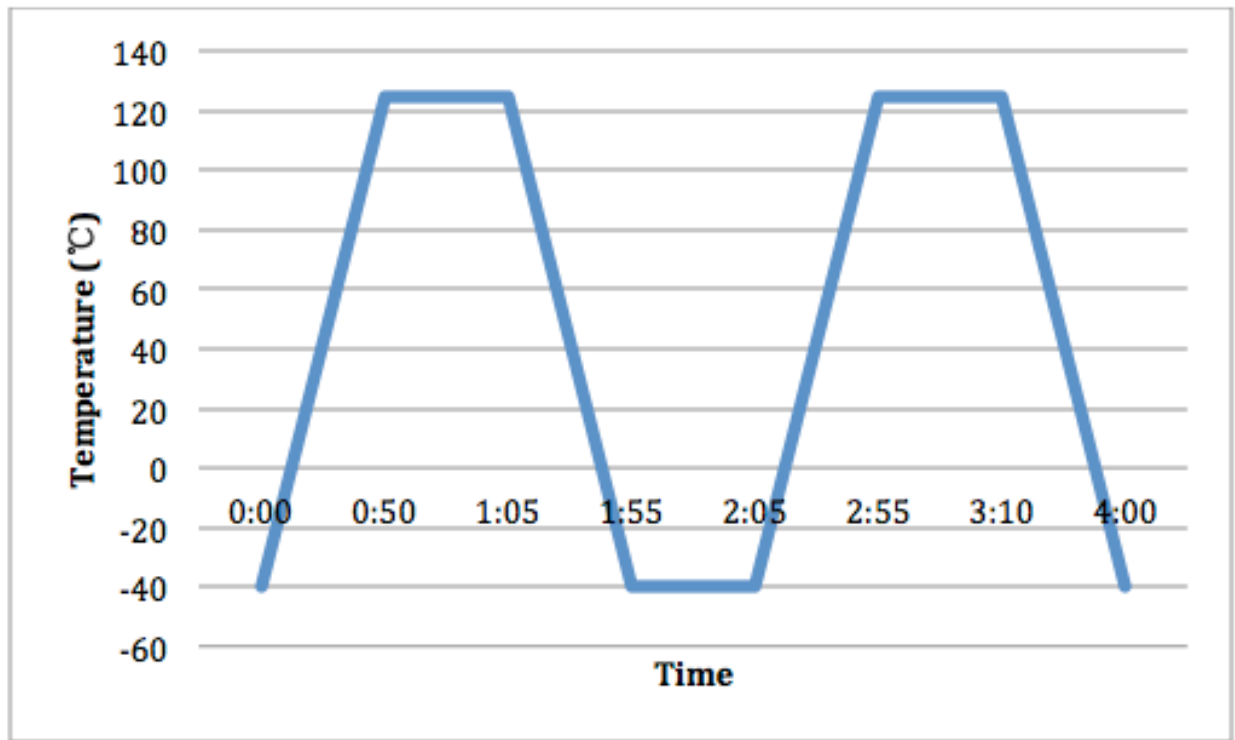


Figure 3.7 Thermal cycling test profile

3.3.2 Data Acquisition System

Inside the thermal cycling chamber all test vehicles were placed vertically, on top of which daisy-chained components were wired out to a data acquisition system developed by Dr. Thomas Sanders of Auburn University. This system consists of a Keithley 7002 switch scanning system coupled with a high accuracy Keithley 2001 digital multi-meter, which allows for continuously monitoring the resistance change of each component. This system was all controlled automatically by LabView software. Based on IPC-9701 standard, the practical definition of solder joint failure is an interruption of electrical continuity > 1000 Ohms. In this study, we defined “failure” to occur when the daisy chain resistance increased (from baseline) by over 100 ohms for 5 sequential resistance measurements. Figure 3.8 shows thermal cycling chamber with

A photograph of a laboratory environment. On the left is a large blue environmental chamber with a viewing window. In the center, a computer monitor sits on a blue metal stand. Below the monitor, on the same stand, is a white electronic device, possibly a power supply or a small environmental test chamber. To the right of the stand is a yellow rolling cart with a black top. In the background, there are more blue equipment units and a black control panel. The floor is a light-colored, polished surface.

(b)

Figure 1: Block diagram of the test system. The diagram illustrates the connection between the Environmental Simulation Chamber and the external test equipment. The chamber wall contains multiple channels (Channel 1 to Channel 40), each with a switch (H/L) and a resistor (R1, R2, R3, ..., R40). These resistors are connected to RTD Temperature Sensors. The sensors are connected to BGA Test Boards. The test boards are connected to 7002 Switching Systems with 7011 Multiplexer Cards. The switching system is connected to a Computer and a Multimeter. A legend indicates the connection types: IEEE-488 (GPIB) (Blue line), Trigger Link (Green line), Output Positive (Red line), Output Negative (Orange line), and Wiring into Chamber (Grey line).



69

3.3.3 Failure Analysis

Test vehicles with failure samples were taken out and cross-sectioned before microscopic examination. Cross-sectioned procedures including a PCB cut by Allied Trim Saw with diamond sectioning blade, following by cold mounting using an epoxy system (resin and hardner). Then grinding was done on a Pace Technologies FEMTO-1000 (with NANO-1000T polishing head) semi-automated polishing machine, with Sic grinding papers of 240, 320, 400, 600, 800, 1200 grit applied in sequence [90]. Finally, the polishing process was performed with 3-micron diamond suspension [91].

Following polishing, the samples were gold sputter coated and examined using scanning electron microscopy (SEM). Backscattered electron (BSE) detection mode was used for cleaner image since the solder joints were metallic samples. Additionally energy-dispersive x-ray spectroscopy (EDX) was done to explore the microstructure and composition of the solder joints. EDX is performed in the SEM using the characteristic x-rays emitted during normal interactions between the electron-beam with samples, returning the elemental composition of a particular section of the solder joint [92].

Chapter 4

Reliability Data Analysis

4.1 Introduction

In this section, we test a full experimental matrix including various selections of solder alloys (SAC105, SAC305, Matched), doped solder pastes, package sizes and pitch sizes, surface finishes (OSP, ImAg, ENIG), isothermal aging time up to 12 months, and isothermal aging temperature up to 125°C, followed by thermal cycling testing from -40°C to 125°C. After thermal cycling, the reliability data were gathered for all test matrices, and two-parameter Weibull analysis and failure percentages were generated for failure data. Where sufficient failure data is available, the two-parameter (θ , β) Weibull distribution has been used to characterize the reliability of electronic packages. The characteristic life θ is the point (i.e. number of cycles) at which 63.21% of the population is expected to fail and the slope β relates to the variance of the data and helps distinguish different failure modes. The least squares method was used to estimate the θ and β values of the Weibull distribution, and the r^2 value indicates the quality of the data fit. Data collection for this project is ongoing, and until the publication of this dissertation, 2700 thermal cycles have been run.

4.2 Data Analysis

4.2.1 Failure Percentage

Table 4.1 and Table 4.2 show the available package failure percentage data based on surface finish and solder material/mixing. As we mentioned, at time of writing, 2700 thermal cycles have been run. For each specific surface finish with doped solder paste, the number of test vehicles are 5, which means for each surface finish/doped solder paste combination, we have 5 samples or data points for each package on the test vehicle. At 2700 thermal cycles, if only 1 test vehicle

with specific surface finish/doped solder paste is recorded to have a particular package failed, then the failure percentage will be 20%. The same, if all 5 test vehicles are recorded to have a package failed, then the failure percentage would be 100%.

Table 4.1 Package failure percentages with aging (2700 thermal cycles)

Component Doped Paste	12 month aging at 125°C											
	OSP				ImAg				ENIG			
	15mm SAC105	15mm SAC305	15mm Match	2512 Resistor	15mm SAC105	15mm SAC305	15mm Match	2512 Resistor	15mm SAC105	15mm SAC305	15mm Match	2512 Resistor
Paste A	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Paste B	100%	60%	100%	0	100%	40%	40%	0	60%	20%	0	0
Paste C	60%	100%	NA	0	40%	40%	NA	0	20%	40%	NA	20%
Paste D	100%	0	80%	0	80%	20%	40%	0	40%	20%	0	0
Paste E	100%	60%	60%	0	100%	20%	40%	0	40%	20%	0	20%
Paste F	100%	40%	0	100%	100%	40%	40%	100%	100%	40%	20%	100%
Paste G	100%	60%	80%	100%	100%	100%	80%	100%	100%	40%	60%	100%
Paste H	100%	60%	NA	0	100%	40%	0	20%	100%	40%	NA	20%
Paste I	100%	100%	100%	100%	100%	40%	100%	100%	100%	60%	100%	100%
Paste J	100%	40%	100%	40%	80%	40%	100%	40%	40%	20%	60%	20%
Paste K	80%	0	NA	0	40%	0	NA	0	80%	100%	NA	0
Paste L	100%	60%	NA	40%	100%	80%	NA	80%	60%	80%	NA	60%

Table 4.2 Package failure percentages without aging (2700 thermal cycles)

Component Doped Paste	No aging											
	OSP				ImAg				ENIG			
	15mm SAC105	15mm SAC305	15mm Match	2512 Resistor	15mm SAC105	15mm SAC305	15mm Match	2512 Resistor	15mm SAC105	15mm SAC305	15mm Match	2512 Resistor
Paste B	80%	0	0	0	60%	0	40%	0	40%	0	40%	0
Paste C	100%	0	NA	0	80%	40%	NA	20%	100%	0	NA	0
Paste K	100%	0	NA	0	100%	0	NA	0	60%	0	NA	20%
Paste M	100%	80%	NA	80%	100%	40%	NA	100%	100%	40%	NA	20%
Paste N	100%	40%	NA	100%	100%	60%	NA	100%	80%	20%	NA	80%

Both Table 4.1 and Table 4.2 only show the failure percentage for the 15mm BGA package and 2512 SMR with and without aging, because no failure occurred for the 6mm BGA and QFN packages across all test groups. This corresponds to the standard DNP scaling relationship and also matches with the previous research by Zhao, et al. [35], which mentioned that the BGA with full array ball arrangement tends to have much higher reliability than perimeter array.

Complete failures (100% failure percentage) are marked with red in the table. Based on Table 4.1, we can conclude that after 2700 thermal cycles, Paste A performs worst for all test components, followed by Paste I, which only performs well with a SAC305 solder sphere BGA. Application of Paste F and Paste G with a SAC105 solder sphere and a 2512 resistor can cause reliability issues. Paste C, Paste D, and Paste K only have 1 complete package failure, so they are the primary candidates for best performance solder paste material. Paste B, Paste E, Paste H, Paste J, and Paste L are also selected as candidates for best material under further investigation. As shown in Table 4.2, we choose 5 solder pastes to be thermal cycled without aging as a comparison to the aging group.

For packages with 100% failure percentage, Weibull plots can be generated for data analysis to obtain characteristic life for reliability. If the failure percentage is only 20%, which means it has only 1 failure data point, then Weibull analysis cannot be conducted. For failure percentage to be 40%, 60%, and 80%, the higher the failure percentage, the more accurate characteristic life will be acquired from Weibull plots.

4.2.2 Weibull Plots and Degradation Charts

4.2.2.1 Reliability Performance of All Solder Pastes

From Table 4.1, it can be found that for solder pastes with OSP surface finish, almost all 15mm BGA package with SAC105 solder sphere have completely failed. So Weibull plot can be generated to investigate the characteristic life. Figure 4.1 shows Weibull plot for the 15mm BGA package with SAC105 solder sphere on all solder pastes with OSP surface finish aged at 125°C for 12 months.

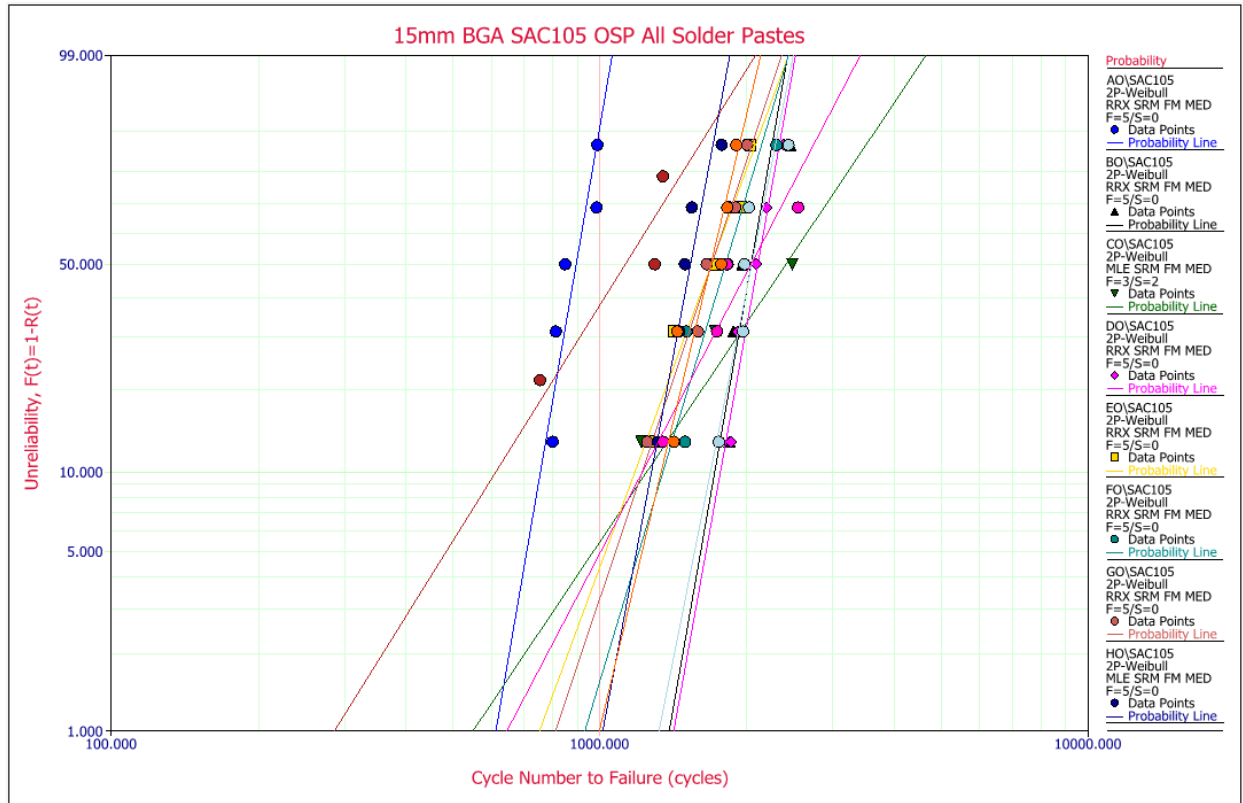


Figure 4.1 Weibull plot for 15mm BGA package with SAC105 solder sphere and OSP surface finish on all solder pastes.

To illustrate the Weibull data more clearly, we construct a characteristic life degradation chart (η vs. solder paste) based on the Weibull plots. Figure 4.2 shows a degradation chart for the 15mm BGA package with SAC105 solder sphere on all solder pastes with OSP surface finish aged at 125°C for 12 months.

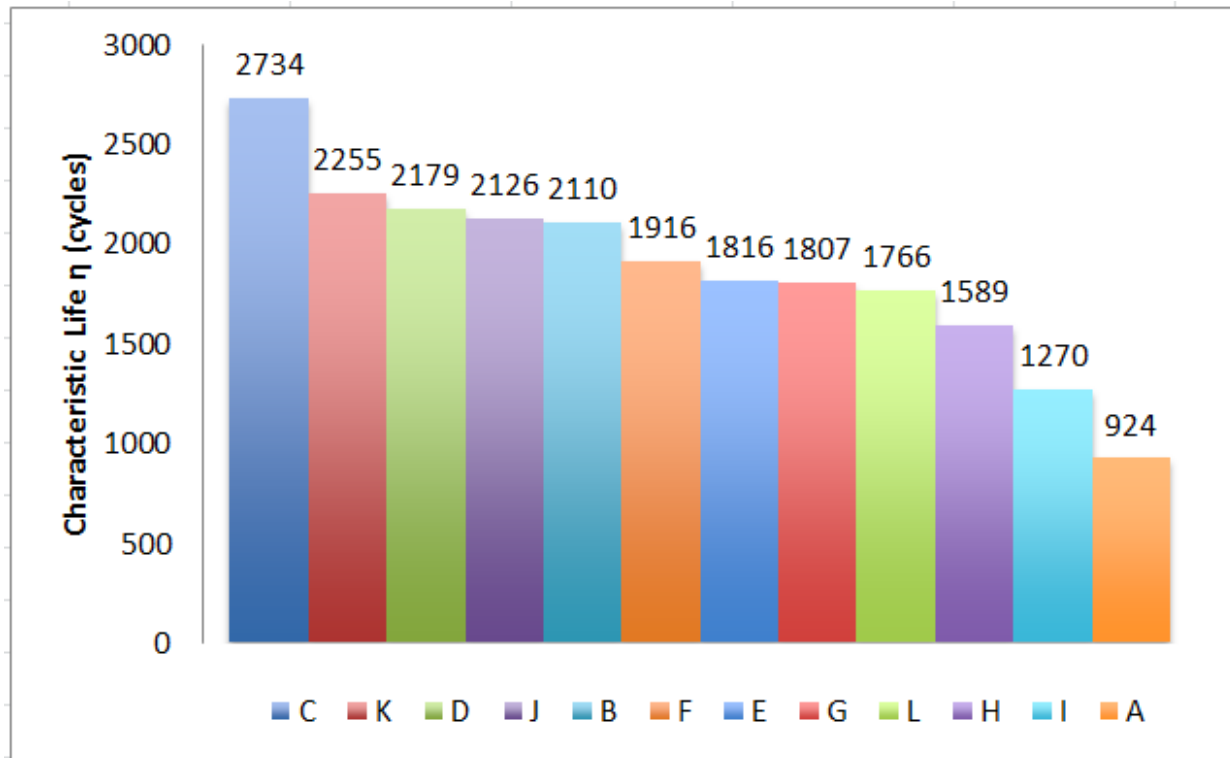


Figure 4.2 Degradation chart for 15mm BGA package with SAC105 solder sphere and OSP surface finish on all solder pastes.

From Figure 4.2 it is readily observed that for the 15mm BGA with SAC105 solder sphere and OSP surface finish aged at 125°C for 12 months, Paste C performs best, followed by Paste K, Paste D, Paste J, and Paste B, which all have a characteristic life over 2000 cycles. Paste A performs worst with a characteristic of 924 cycles. Compared to best performing Paste C, the characteristic life is reduced from 2734 to 924 cycles for Paste A, which is a 66.2% degradation. Besides characteristic life, it's also import to consider B10 life for early failures performance of pastes, by which 10 percent of the populations have failed. Figure 4.3 shows a B10 life degradation chart for the 15mm BGA package with SAC105 solder sphere on all solder pastes with OSP surface finish aged at 125°C for 12 months.

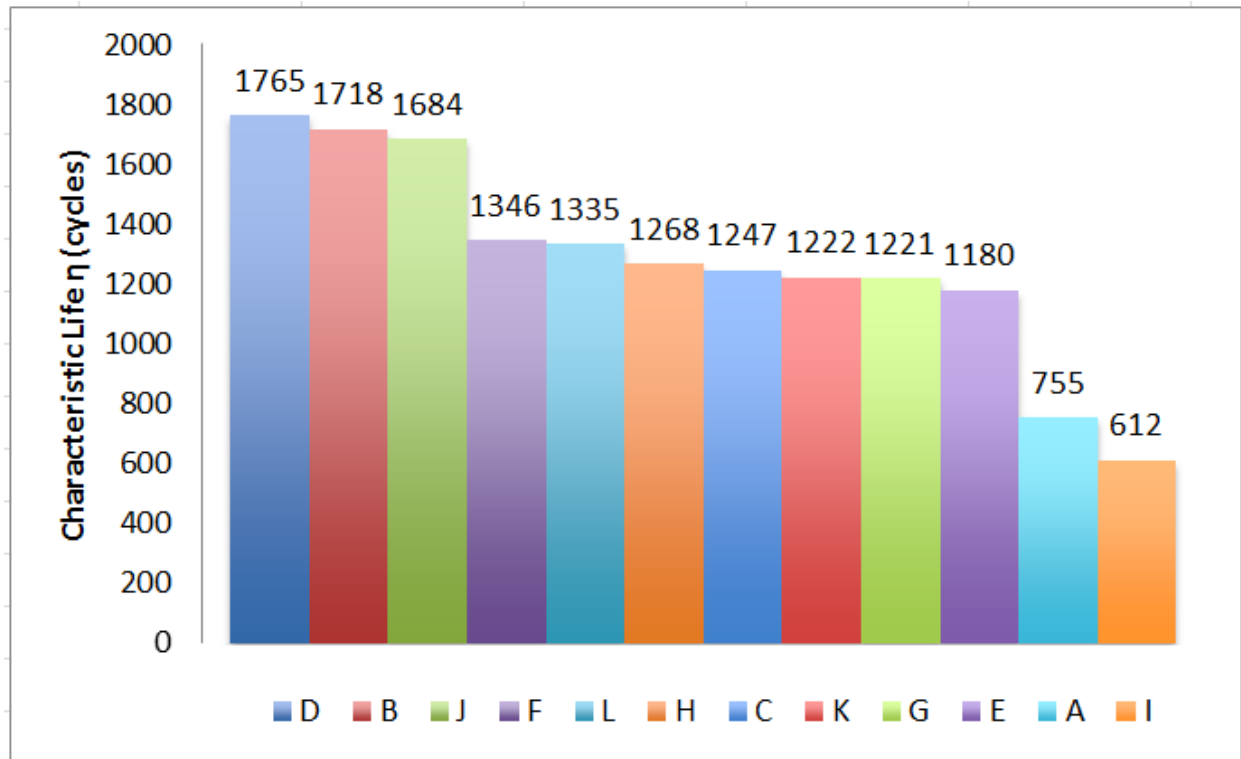


Figure 4.3 B10 life degradation chart for 15mm BGA package with SAC105 solder sphere and OSP surface finish on all solder pastes.

From Figure 4.3, we can conclude that Paste D, Paste B, and Paste J perform better than other solder pastes during early stages. Although Paste C has the best performance of characteristic life, it also has more early failures. Paste A and Paste I perform worse reliability in both characteristic life and early failures.

Similarly, Weibull plots can be generated for the 15mm BGA package with SAC105 solder sphere on all solder pastes with ImAg surface finish aged at 125°C for 12 months is shown in Figure 4.4.

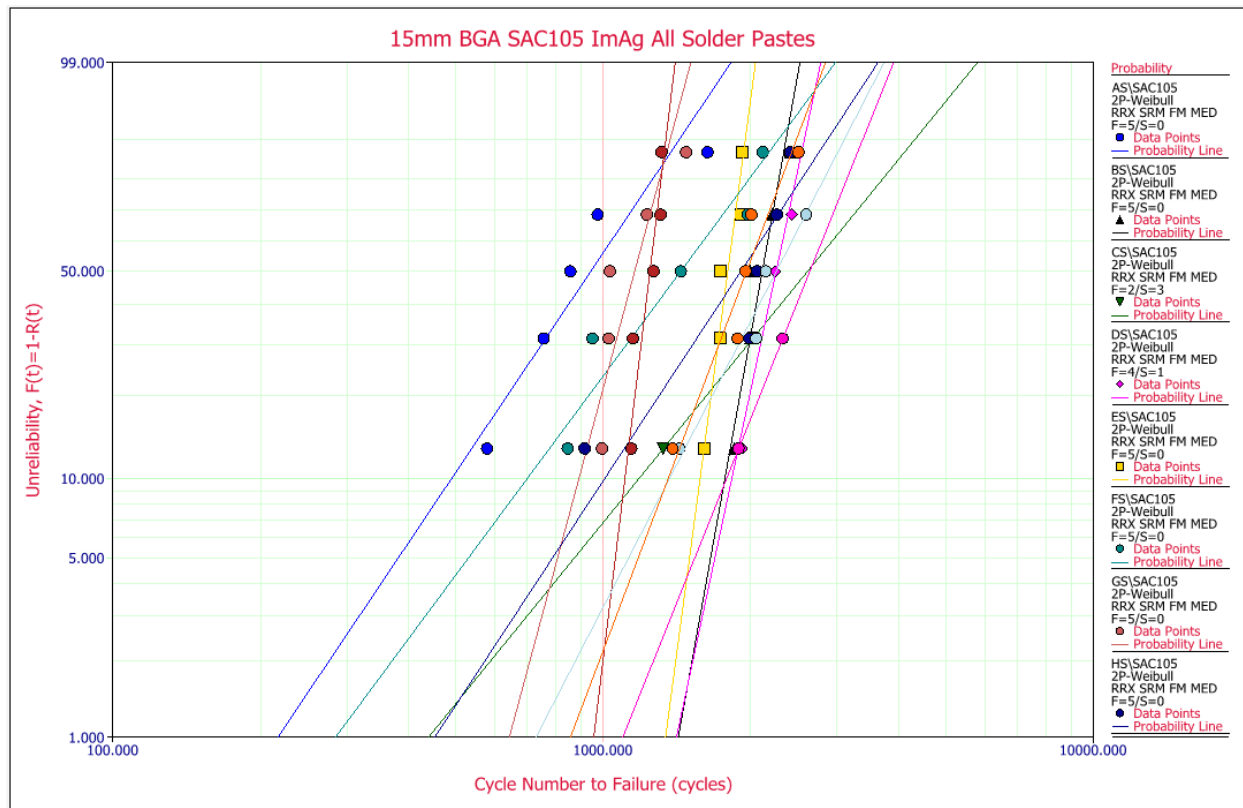


Figure 4.4 Weibull plot for 15mm BGA package with SAC105 solder sphere and ImAg surface finish on all solder pastes.

Based on Figure 4.4, the degradation chart for the 15mm BGA package with SAC105 solder sphere on all solder pastes with ImAg surface finish aged at 125°C for 12 months is shown in Figure 4.5.

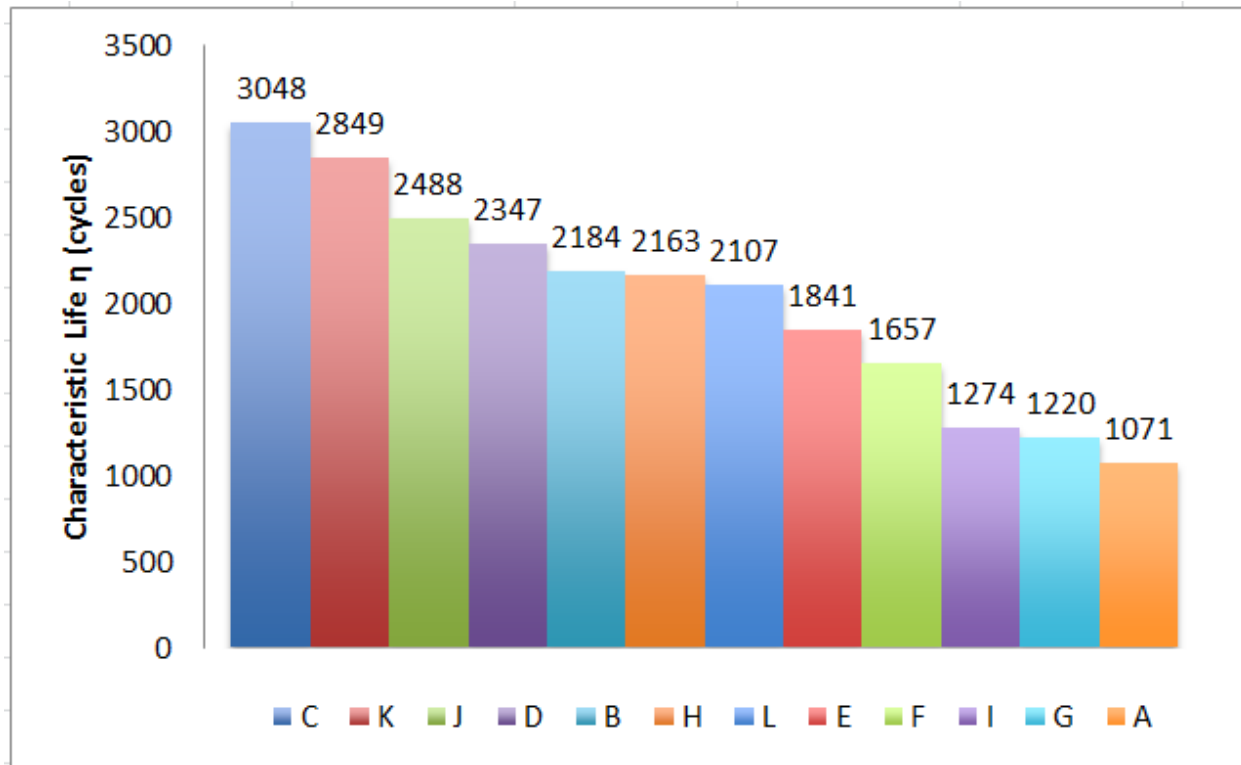


Figure 4.5 Degradation chart for 15mm BGA package with SAC105 solder sphere and ImAg surface finish on all solder pastes.

Figure 4.5 demonstrates that for the 15mm BGA with SAC105 solder sphere and ImAg surface finish aged at 125°C for 12 months, again Paste C performs best, followed by Paste K, Paste J, Paste D, and Paste B. Paste H and Paste L also have a characteristic life over 2000 cycles at this time. Paste A again performs worst with a characteristic life of 1071 cycles. Compared Paste C, the characteristic life is reduced from 3048 to 1071 cycles for Paste A, which is a 64.9% degradation.

Figure 4.6 shows the B10 life degradation chart for the 15mm BGA package with SAC105 solder sphere on all solder pastes with ImAg surface finish aged at 125°C for 12 months.

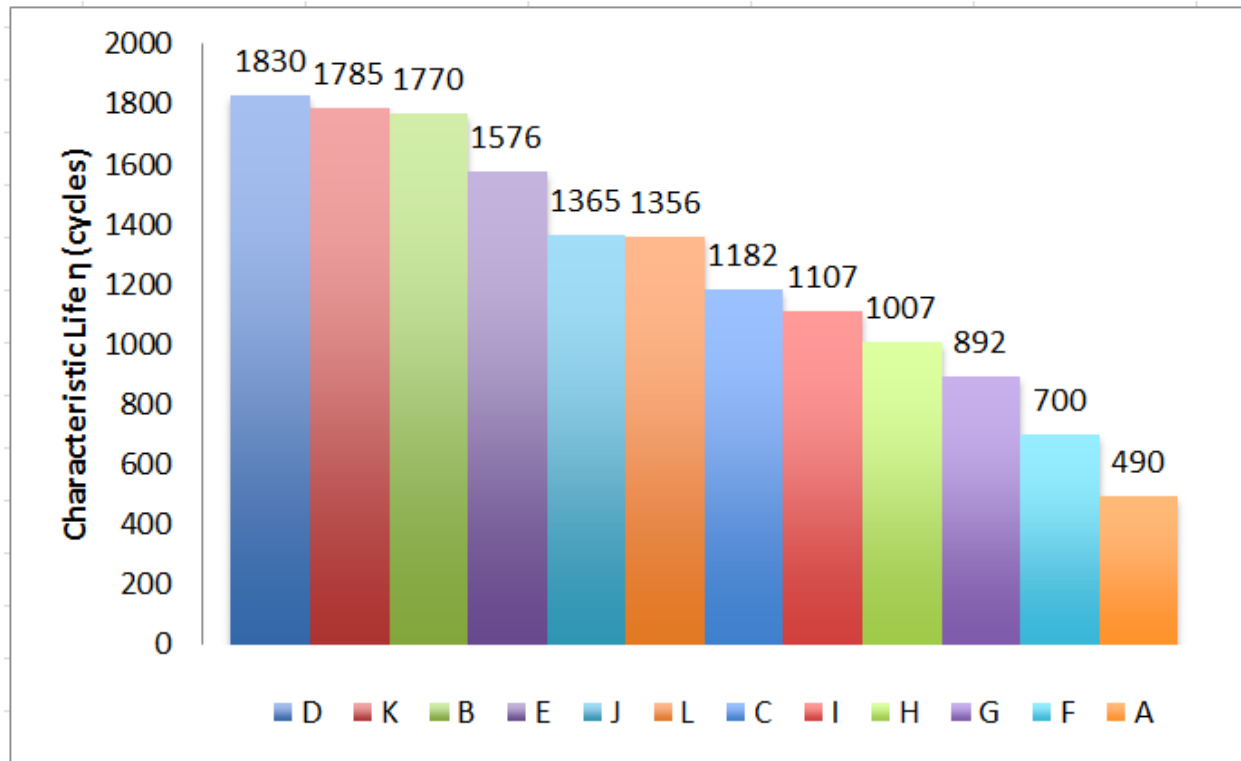


Figure 4.6 B10 life degradation chart for 15mm BGA package with SAC105 solder sphere and ImAg surface finish on all solder pastes.

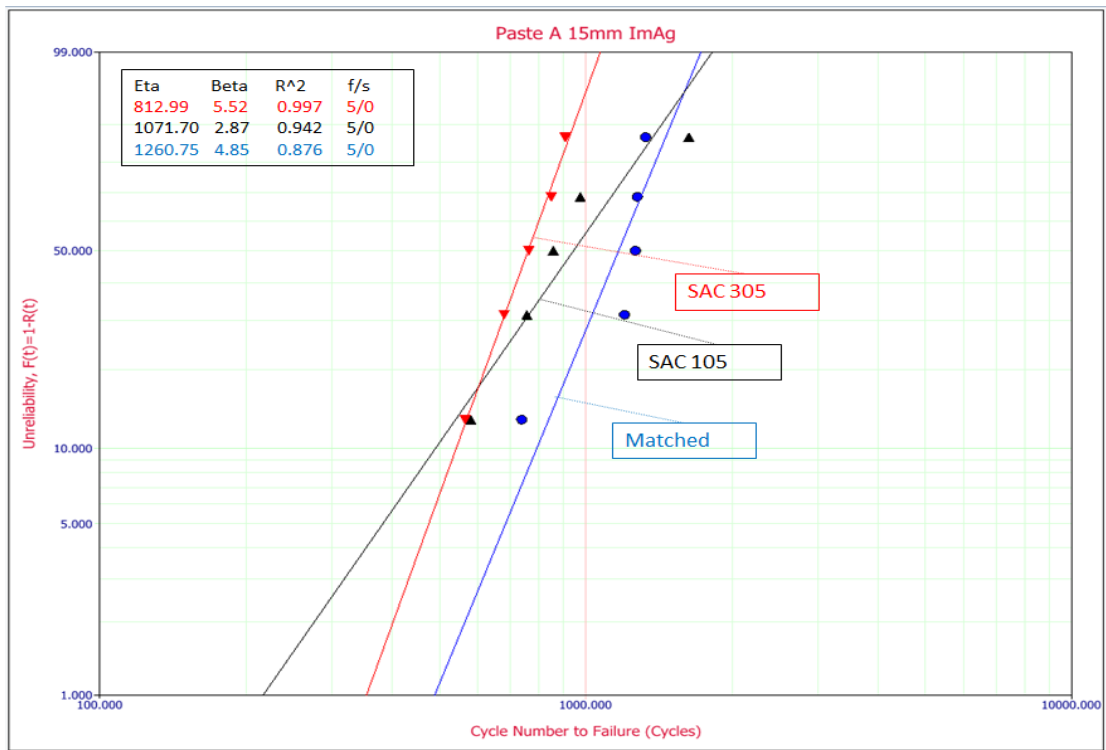
From Figure 4.6, we can conclude that for ImAg surface finish, Paste D, Paste K, and Paste B perform better than other solder pastes during early stages. Recall from Figure 4.3, which shows for OSP surface finish, Paste D, Paste B, and Paste J have better reliability in early life. So we may conclude that applying Paste D or Paste B can improve early life reliability. Again, for ImAg surface finish, Paste A performs the worst in both characteristic life and early failures.

As mentioned in section 4.2.1, Table 4.1 shows that Paste C, Paste D, and Paste K are primary candidates for best performance solder paste materials, which correspond to the Weibull characteristic life shown in Figure 4.2 and Figure 4.5. According to Table 3.2, Paste C, Paste D, and Paste K all have high Ag content ($>3.4\%$), high Bi content ($>3.0\%$), and Sb content ($>1.5\%$).

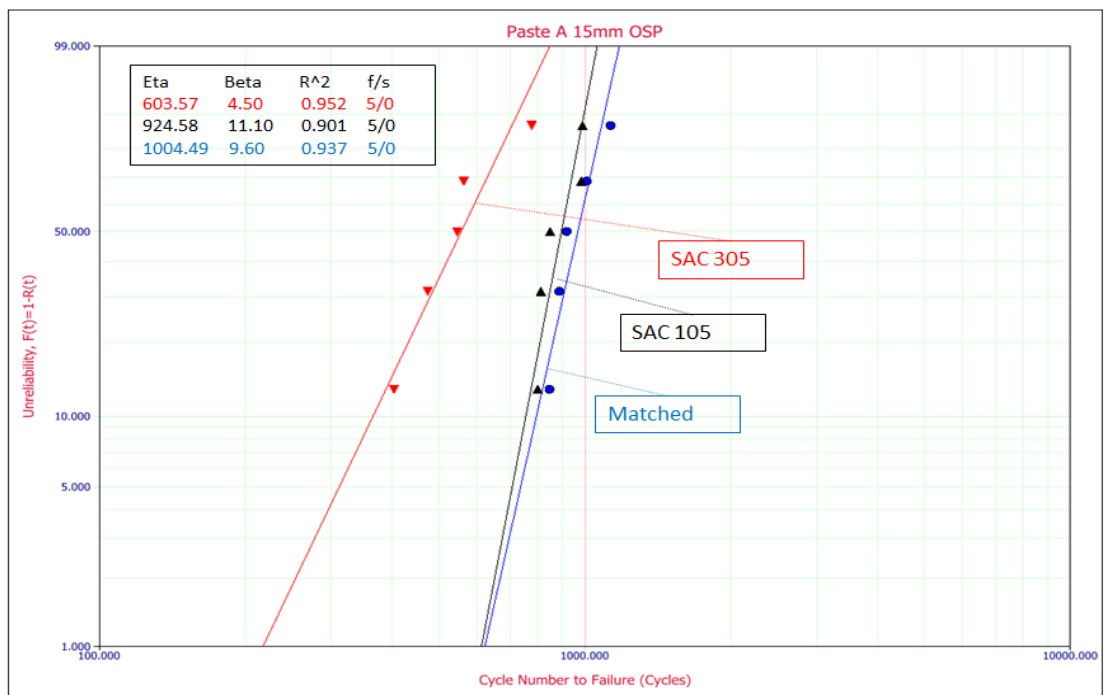
Paste A performs worst for all test components, because it contains very little Ag (0.5%), no Bi and Sb. So Bi and Sb dopants added in SAC alloy can help improve the overall solder joint reliability. We see from Table 3.2 that both Paste K and Paste L are from Henkel company, and both of them contain exactly the same composition. But Paste K performs much better than Paste L. The reason could be for Paste K, it has a particle size of Type 3 (25-45 microns), and in contrast, Paste L has a particle size of Type 4 (20-38 microns). So solder pastes with different particle sizes would have an effect on the reliability of solder joint. Failure analysis will be conducted in Chapter 5 to explain how dopants can affect the microstructure of solder joint and hence influence its reliability.

4.2.2.2 Reliability for BGA Package with Different Solder Spheres

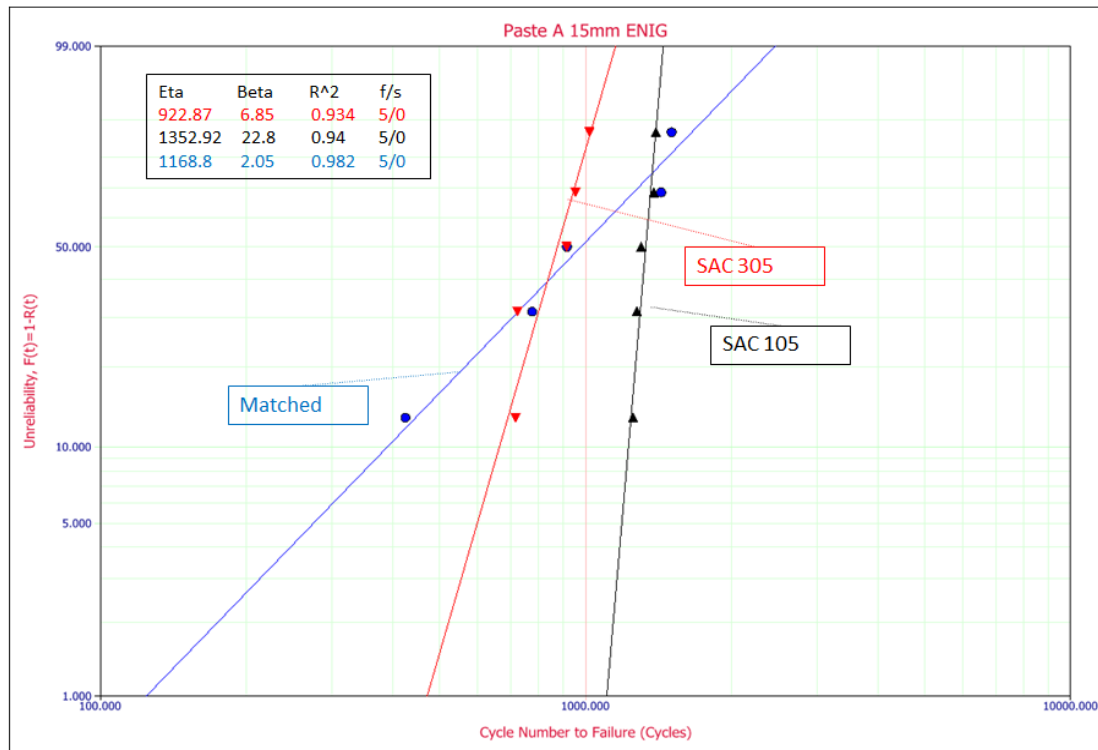
BGA components are mounted on the PCB using second-level interconnects (solder joints). Before being placed on printed solder paste on top of PCB copper pad, BGA packages are pre-balled by SAC105, SAC305 and matched solder sphere, which implies that the spheres of the package have the same composition of printed paste on the PCB. It's useful to consider how different solder spheres can affect the solder joint reliability. Figure 4.7 shows Weibull plots for the 15mm BGA with Paste A after aging on each surface finish considering solder sphere effect.



(a)



(b)



(c)

Figure 4.7 Weibull Plots for the 15mm BGA with paste A after aging on each surface finish: (a) ImAg surface finish, (b) OSP surface finish, (c) EING surface finish

To present the data more succinctly, we have summarized the characteristic life values based on the Weibull fittings. Figure 4.8 shows the characteristic life values for the 15mm BGA with Paste A.

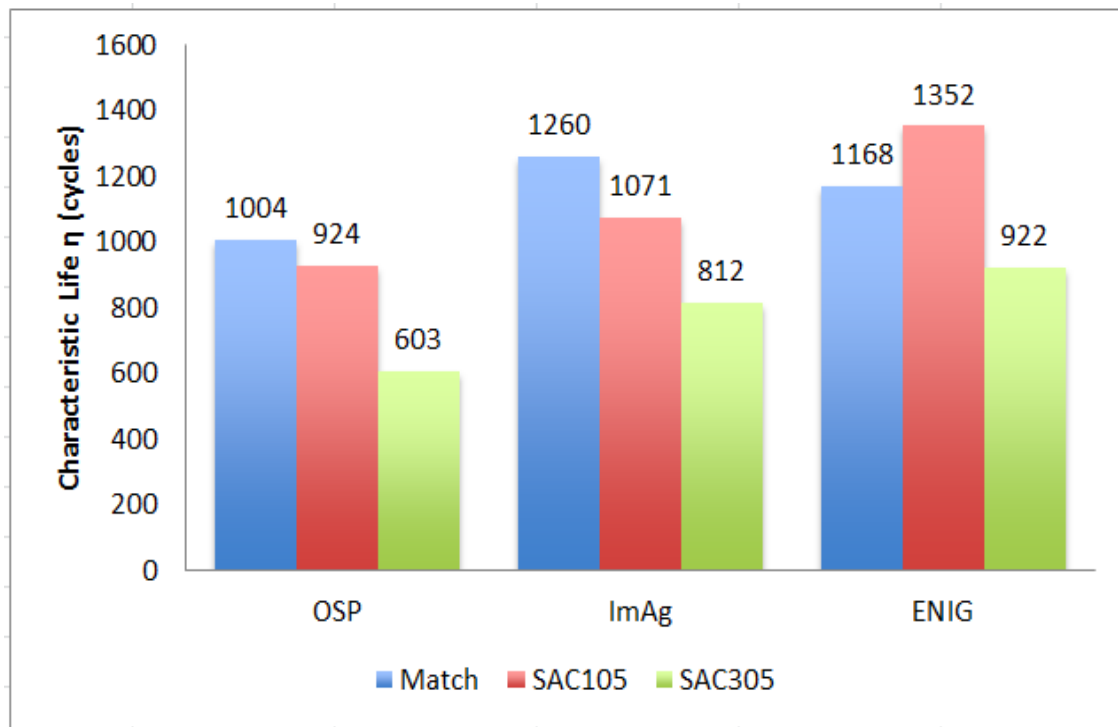
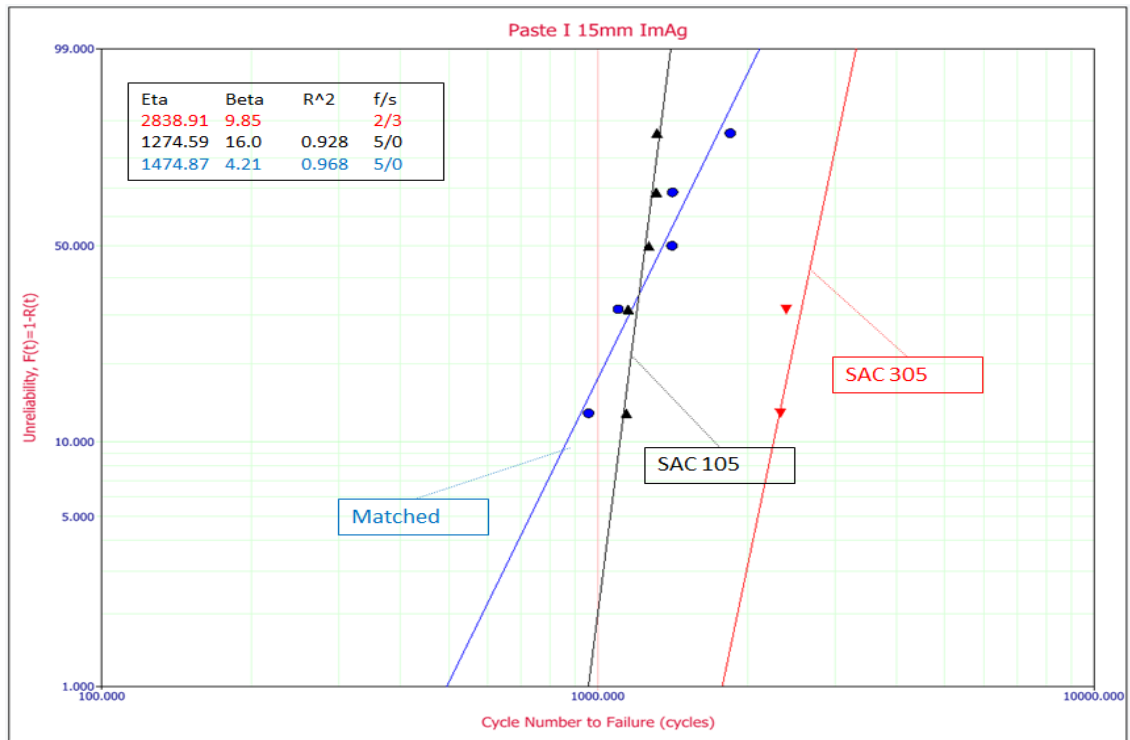


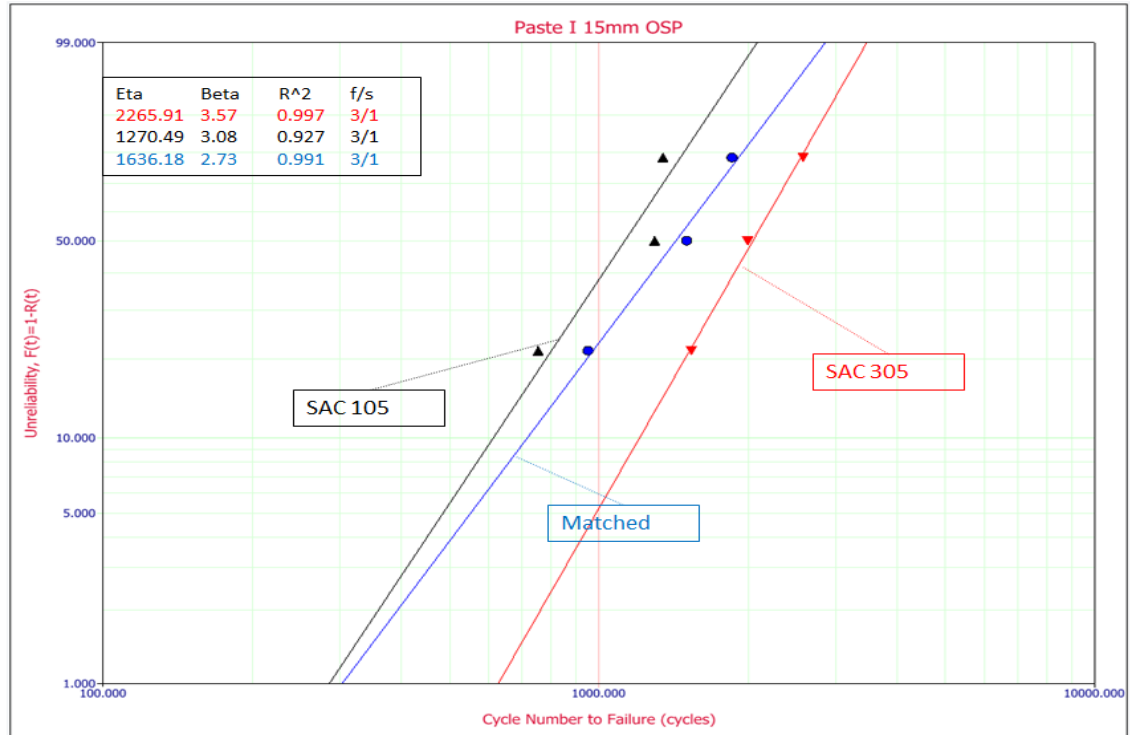
Figure 4.8 Characteristic life values for 15mm BGA with paste A

From Figure 4.8, we can conclude that for Paste A, the matched composition joints perform generally better (with an exception for the ENIG finish) than paste-doped SAC105 and SAC305 joints. Considering paste doping of SAC105 and SAC305, for material A, doped SAC105 joints always outperform doped SAC305 joints. Doped SAC305 joints are found to have lower characteristic life than both the matched Material A joints and doped SAC105 joints in all cases.

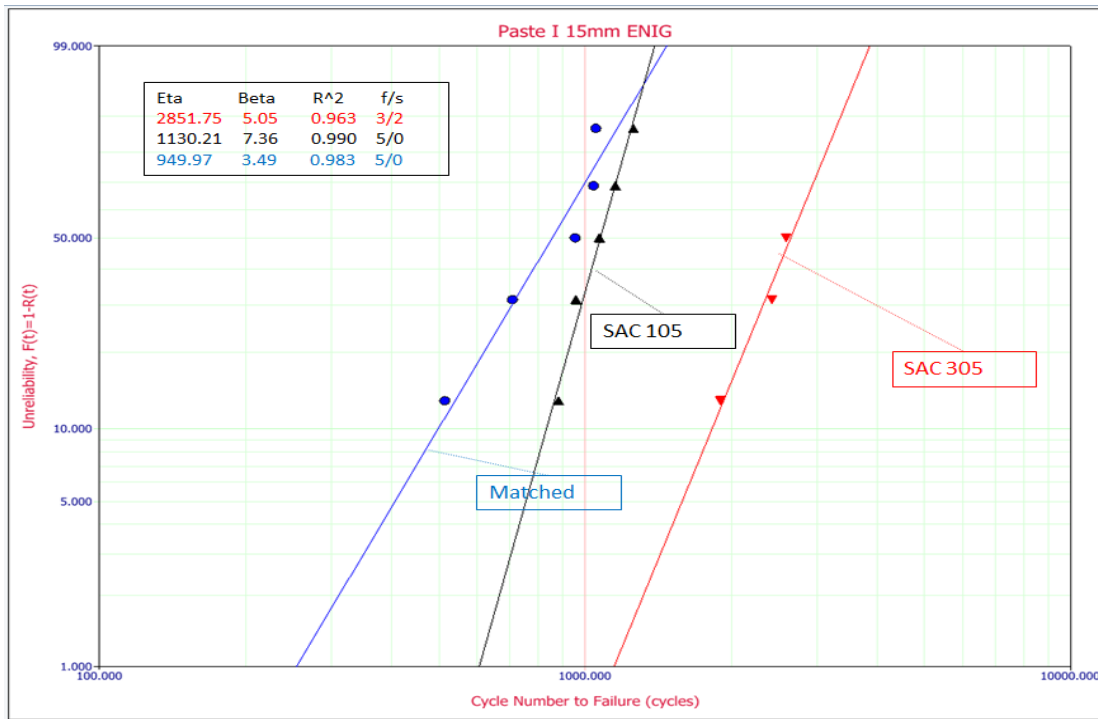
Figure 4.9 shows Weibull plots for the 15mm BGA with Paste I after aging on each surface finish considering solder sphere effect. Figure 4.10 shows the characteristic life values for the 15mm BGA with Paste I.



(a)



(b)



(c)

Figure 4.9 Weibull plots for the 15mm BGA with paste I after aging on each surface finish: (a) ImAg surface finish, (b) OSP surface finish, (c) EING surface finish

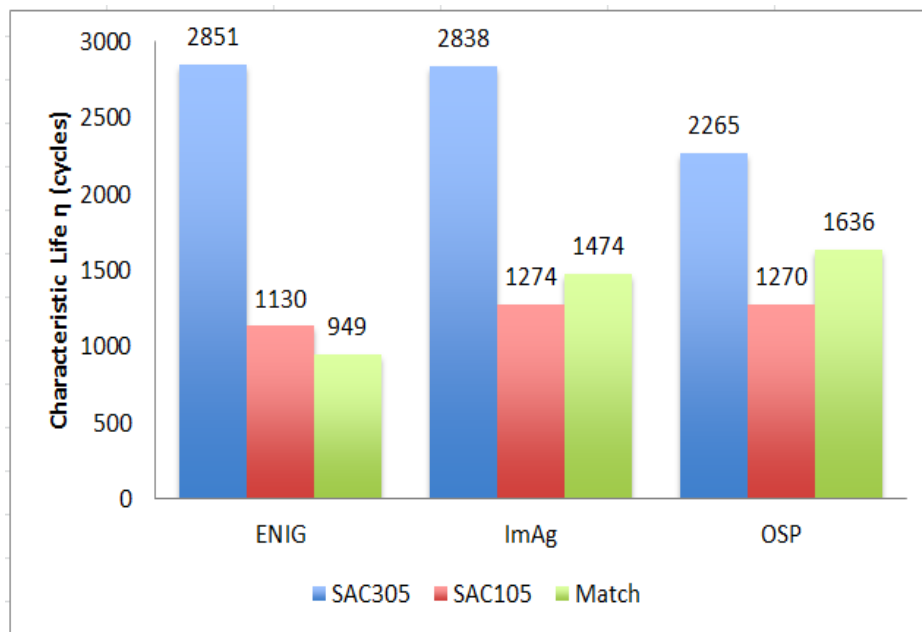
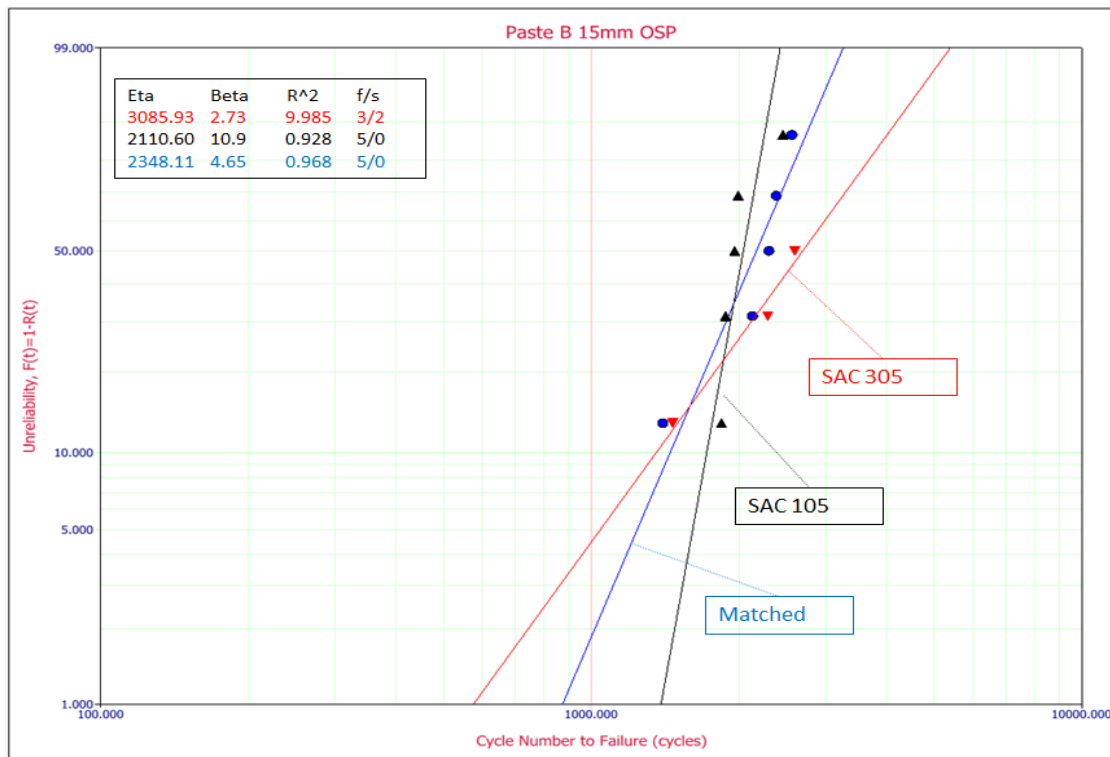


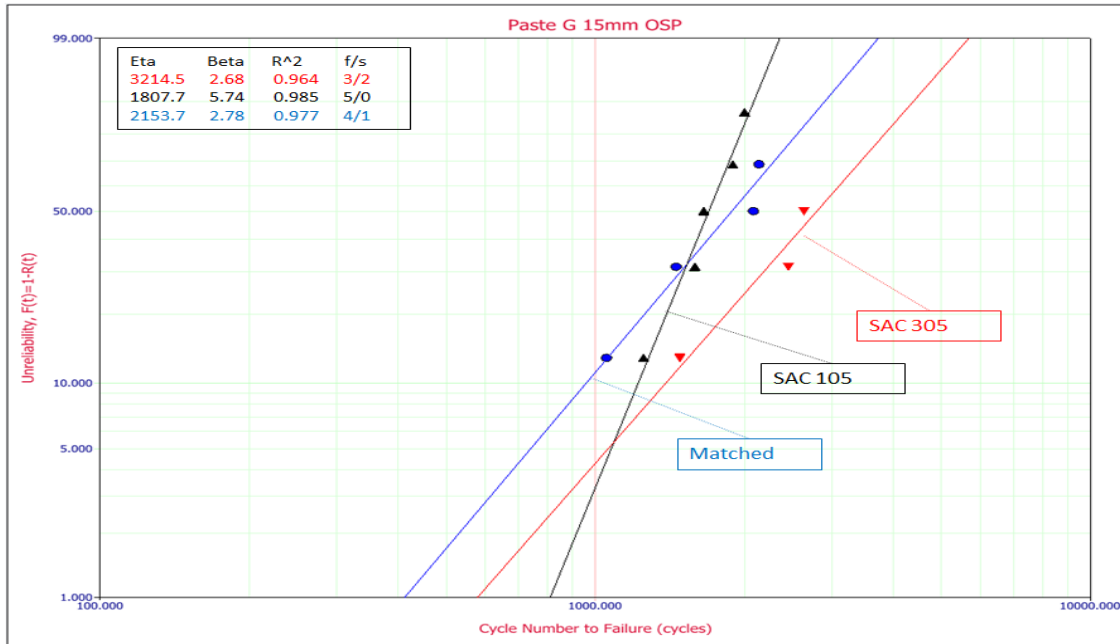
Figure 4.10 Characteristic life values for the 15mm BGA with Paste I

From Figure 4.10, we can conclude that for Paste I, paste-doped SAC305 joints always perform better than paste-doped SAC105 and matched joints. For ImAg and OSP surface finish, matched joints have higher reliability than SAC105, but for ENIG finish SAC105 performs better than matched joint.

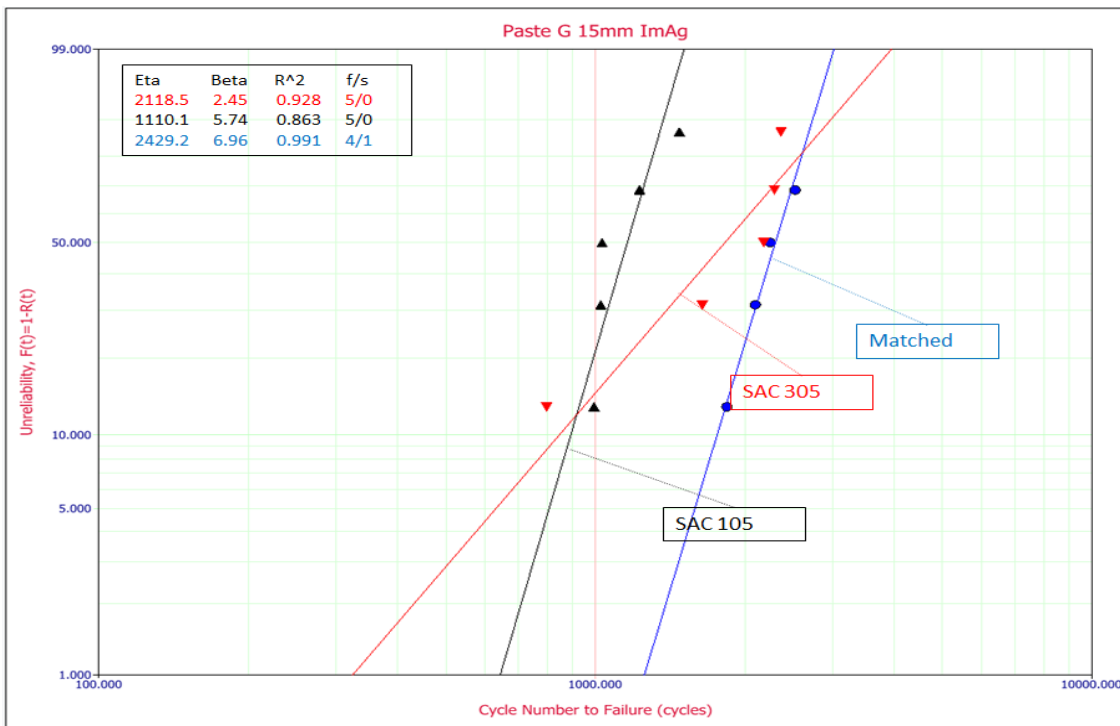
If we refer to Table 4.1, we find Paste B with OSP finish, Paste G with OSP finish, and Paste G with ImAg finish, failure percentages for all of those components are over 60% so that we can generate Weibull analysis. Figure 4.11 shows Weibull plots for the 15mm BGA with Paste B & OSP finish, Paste G & OSP finish, and Paste G & ImAg finish after aging considering solder sphere effect. Figure 4.12 shows the characteristic life values for the 15mm BGA with Paste B & OSP finish, Paste G & OSP finish, and Paste G & ImAg finish.



(a)



(b)



(c)

Figure 4.11 Weibull plots for the 15mm BGA with (a) Paste B & OSP finish, (b) Paste G & OSP finish, (c) Paste G & ImAg finish

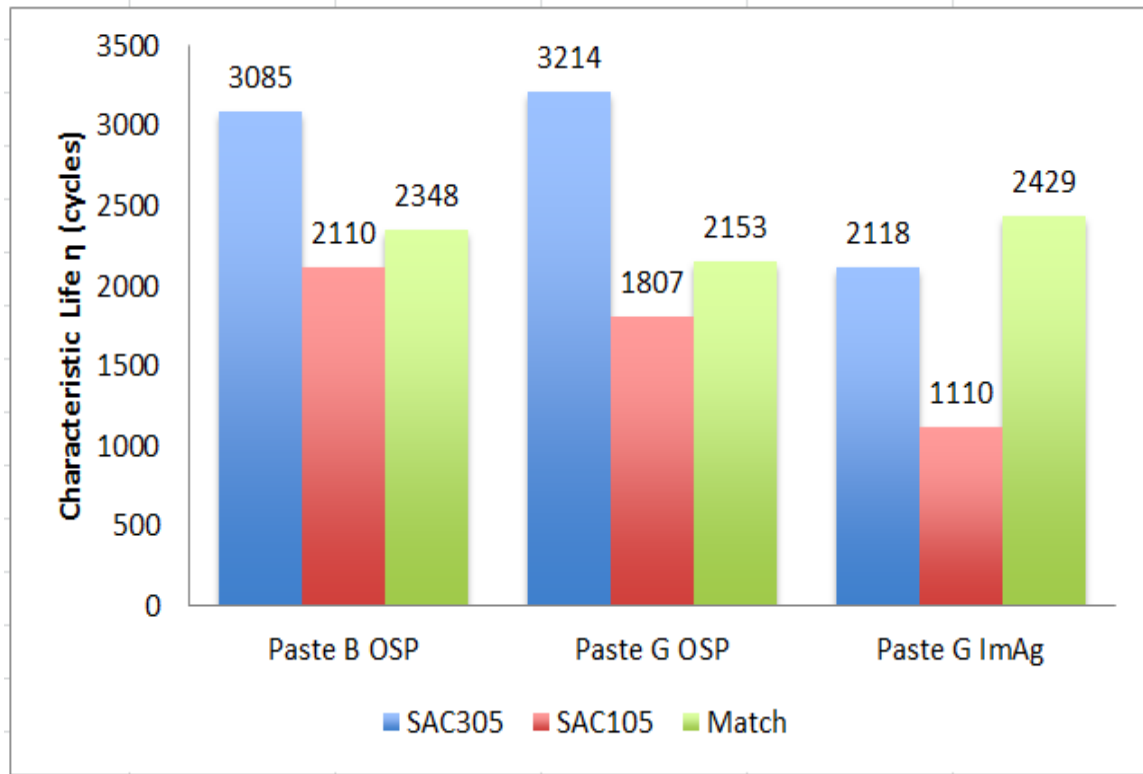
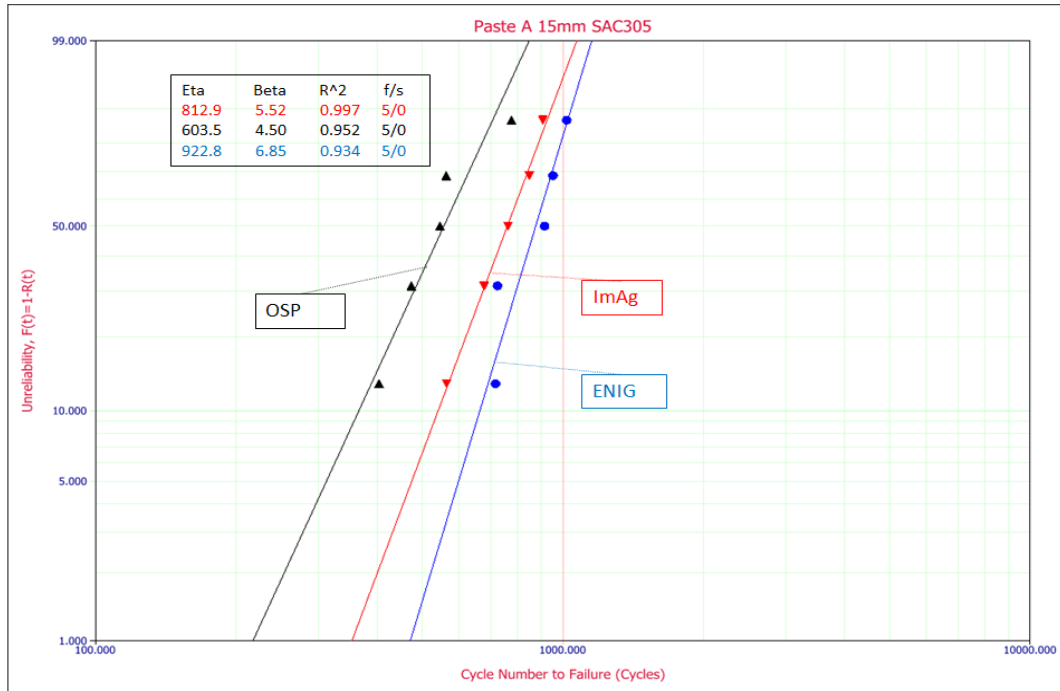


Figure 4.12 Characteristic life values for the 15mm BGA with Paste B & OSP finish, Paste G & OSP finish, and Paste G & ImAg finish

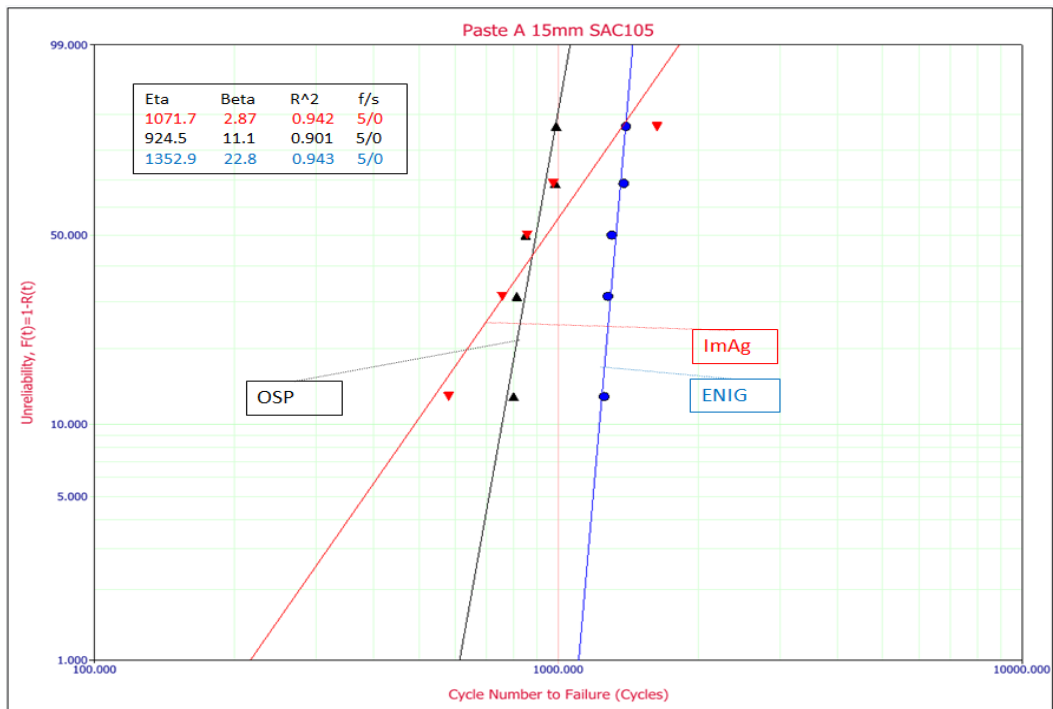
From Figure 4.12 we can observe that for Paste B & OSP finish, paste-doped SAC305 joints perform better than paste-doped SAC105 and matched joints. For Paste B & OSP finish, paste-doped SAC305 joints perform better than paste-doped SAC105 and matched joints. For Paste B & ImAg finish, matched joints have higher reliability than SAC305 and SAC105.

4.2.2.3 Reliability for BGA Package with Different Surface Finishes

Previous research by Hai [93] has shown that ENIG surface finishes inhibit the growth of board-side IMC layers and improve the reliability of BGA components when using SAC105 and SAC305 solder materials. So it's necessary to consider how different surface finishes can have an effect on the solder joint reliability. Figure 4.13 shows Weibull plots for the 15mm BGA with Paste A after aging considering surface finishes effect.



(a)



(b)

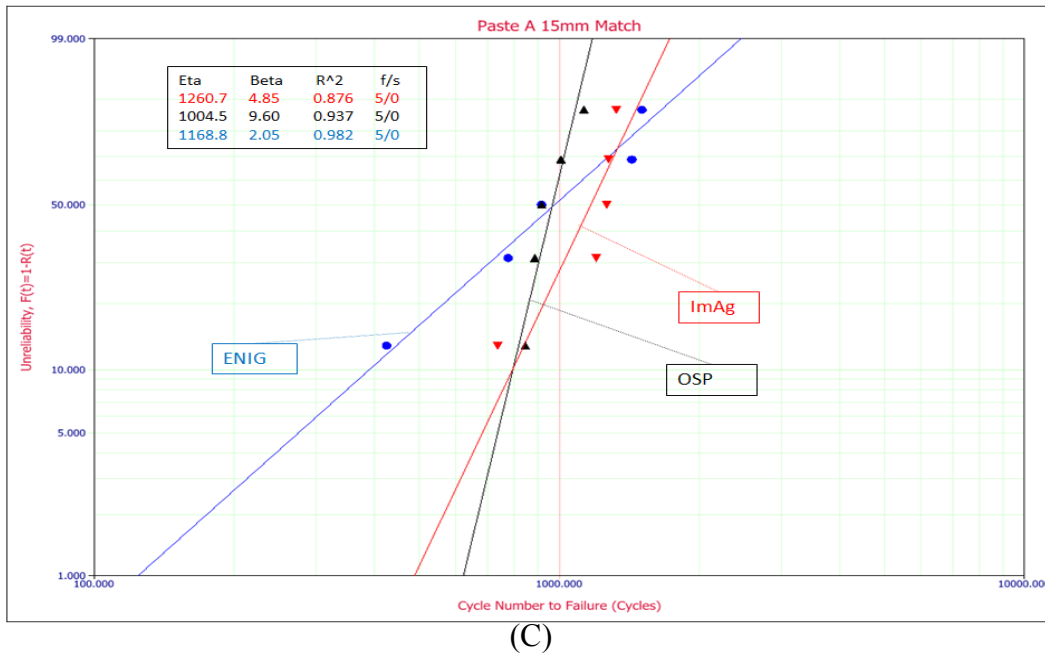


Figure 4.13 Weibull plots for 15mm BGA with Paste A on each surface finish for (a) matched paste and spheres, (b) Paste A with SAC105 spheres, (c) Paste A with SAC305 spheres

We present the characteristic life values based on Weibull analysis for the 15mm BGA with Paste A on each surface finish in Figure 4.14.

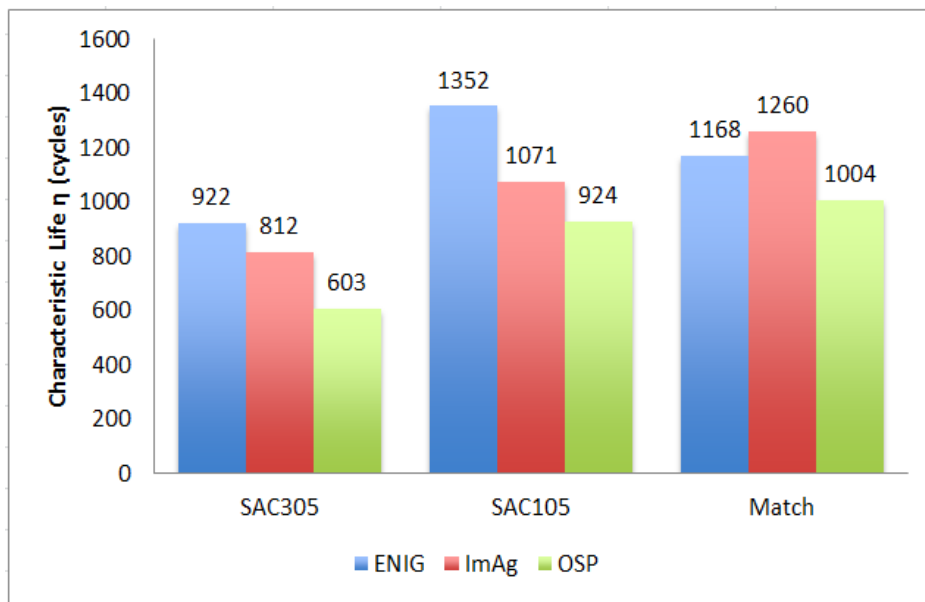
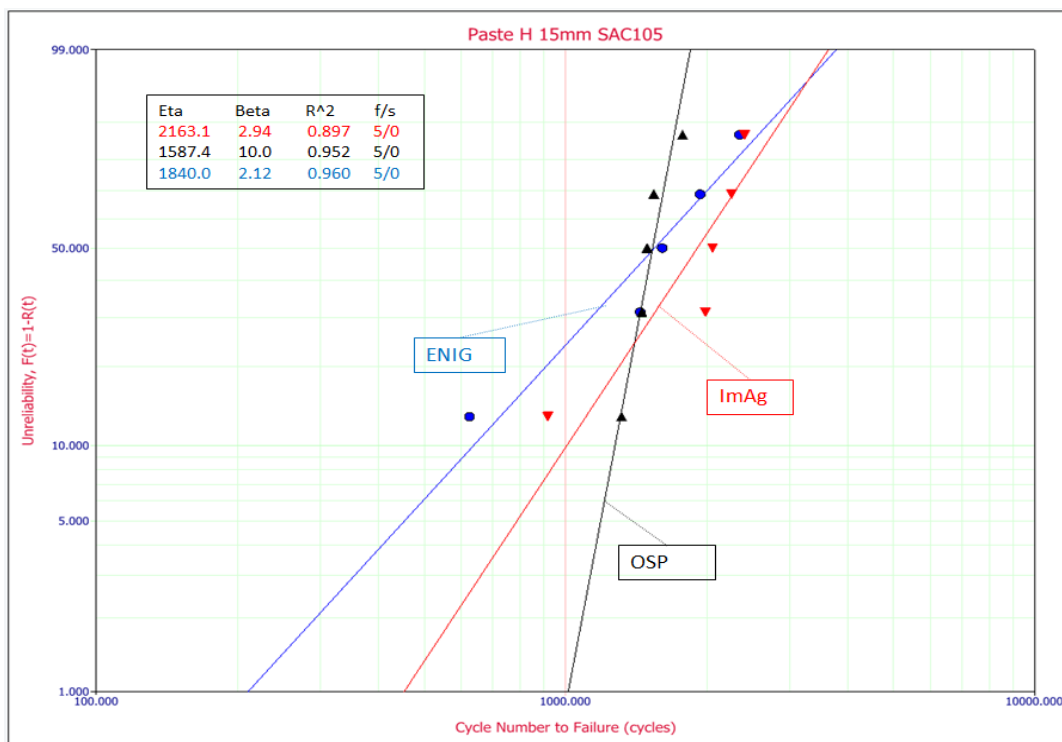


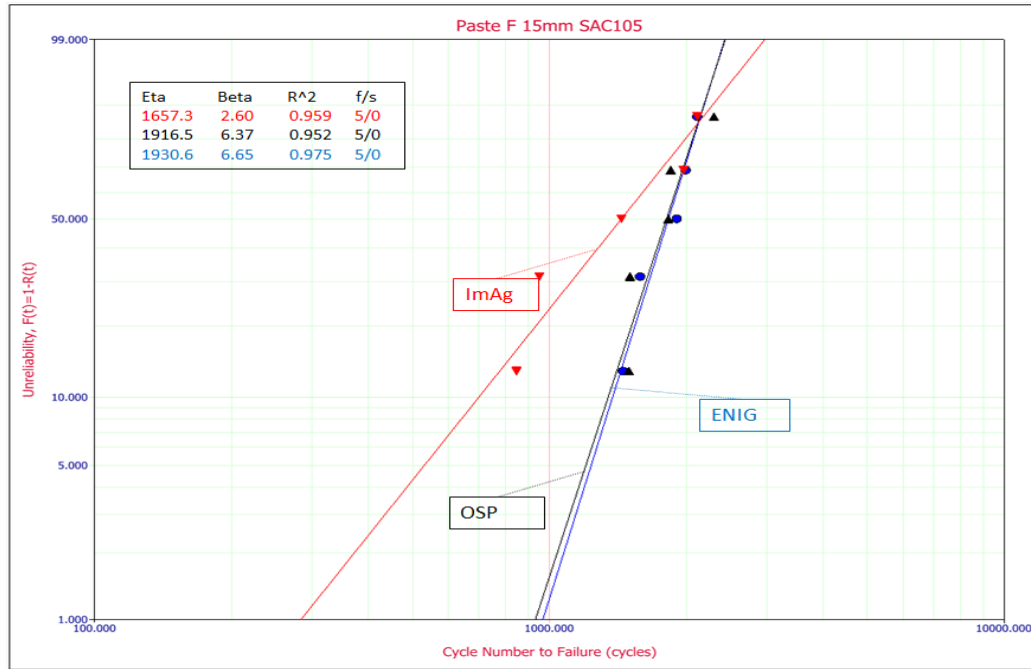
Figure 4.14 Characteristic life values For 15mm BGA with Paste A on each surface finish

Figure 4.14 shows that SAC105 and SAC305 doped with Paste A exhibit similarly enhanced reliability with ENIG surface finishes, as compared to OSP and ImAg finishes. For matched joint, ImAg surface finish has the best reliability. OSP surface finish always performs worst.

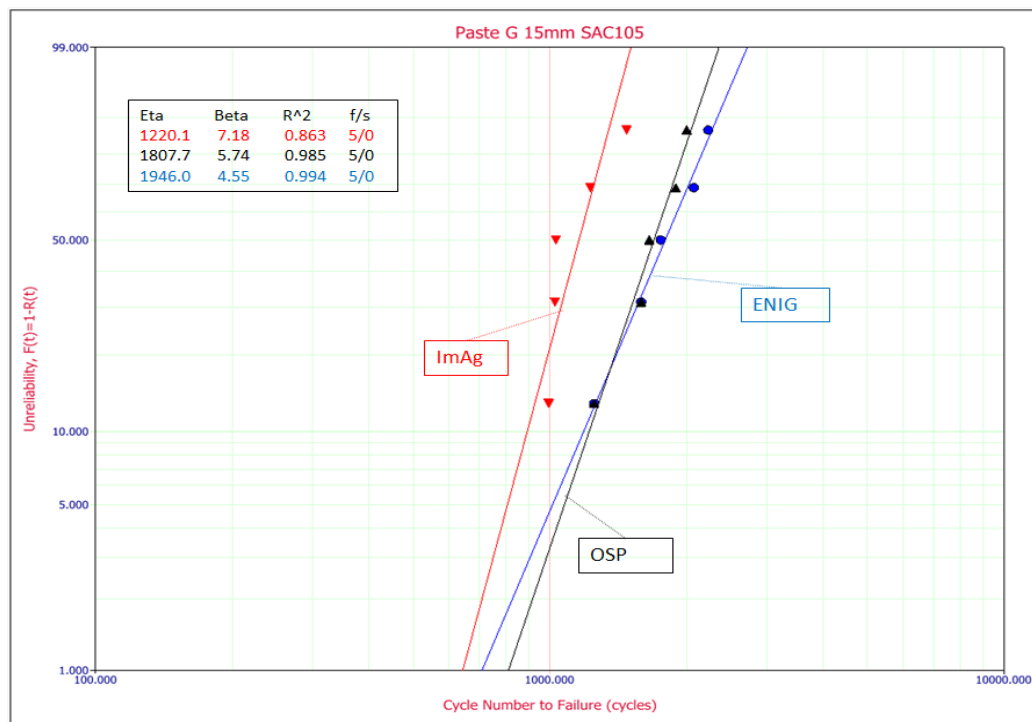
Figure 4.15 shows Weibull plots for 15mm BGA SAC105 sphere with Paste F, Paste G and Paste H after aging considering surface finishes effect. Figure 4.16 shows the characteristic life values for the 15mm BGA SAC105 sphere with Paste F, Paste G and Paste H.



(a)



(b)



(c)

Figure 4.15 Weibull plots For 15mm BGA with SAC105 sphere on each surface finish for (a)

Paste H, (b) Paste F, (c) Paste G

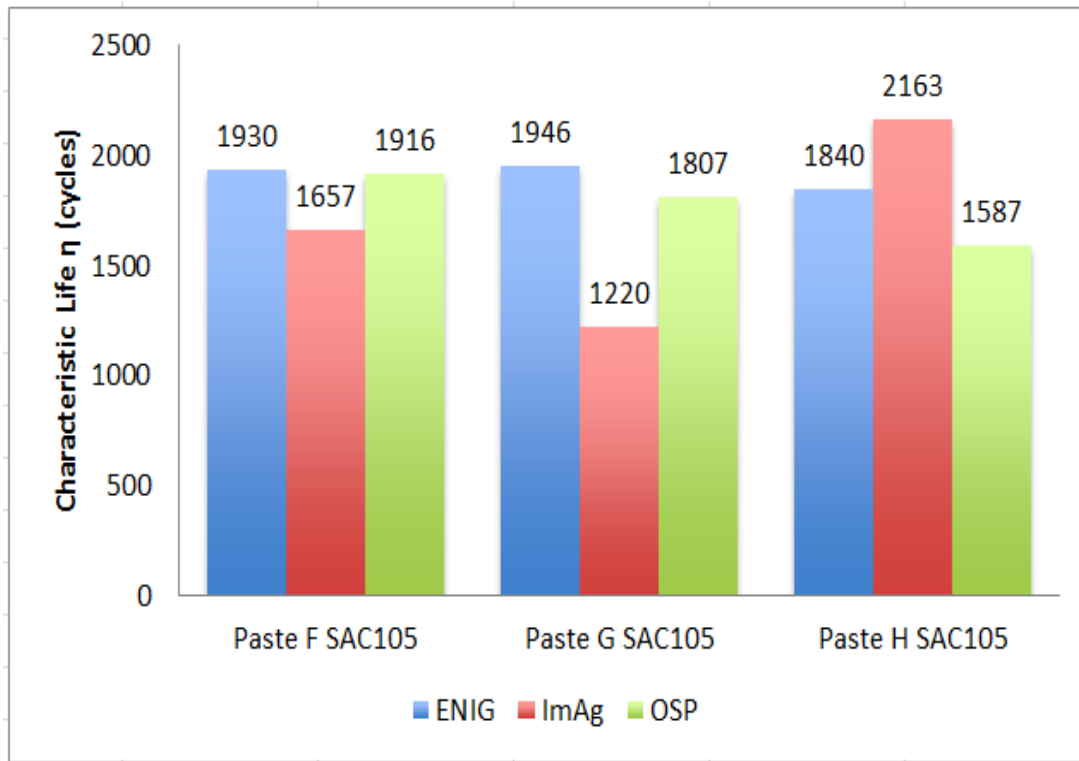
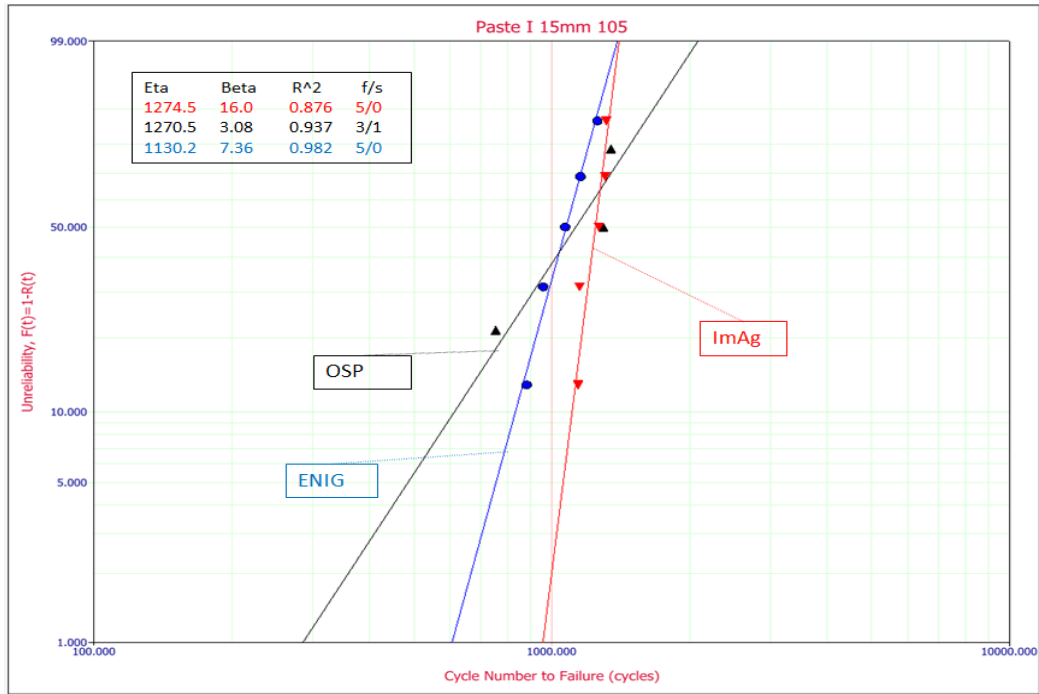


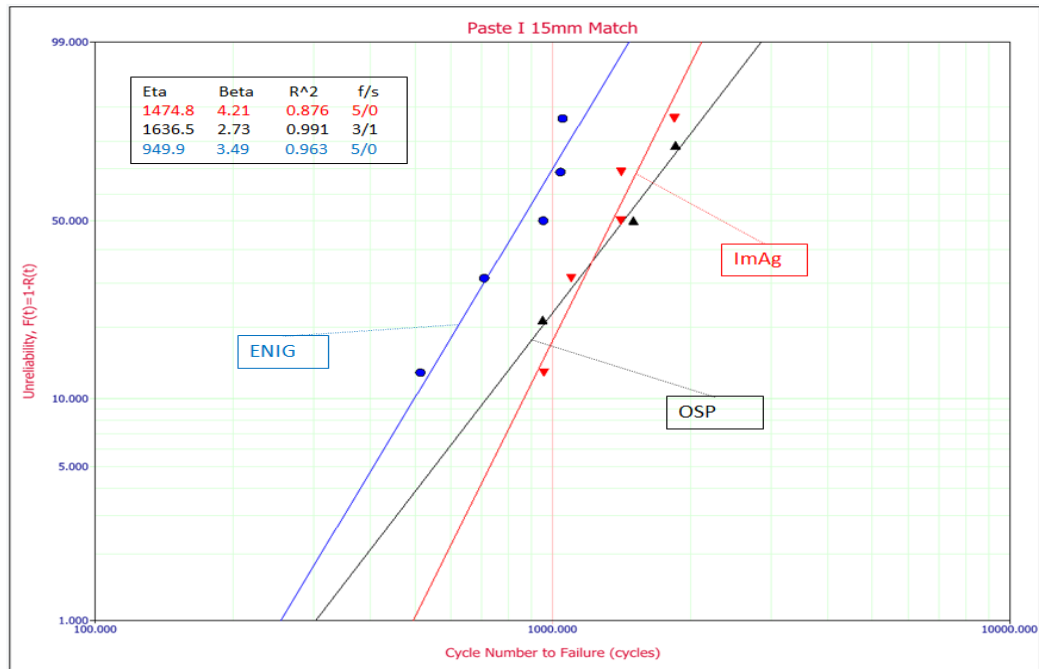
Figure 4.16 Characteristic life values for 15mm BGA SAC105 sphere with Paste F, Paste G and Paste H

From Figure 4.16 we can conclude that for Paste F with SAC105 sphere and Paste G with SAC105 sphere, ENIG surface finish has the best reliability, followed by OSP, while ImAg performs worst. For Paste H with SAC105 sphere, ImAg surface finish has the best reliability, and OSP performs worst.

Similarly, we can obtain Weibull plots for the 15mm BGA with Paste I after aging considering surface finishes effect, which is shown in Figure 4.17. Figure 4.18 shows the characteristic life values for the 15mm BGA with Paste I.



(a)



(b)

Figure 4.17 Weibull plots for 15mm BGA with Paste A on each surface finish for (a) Paste I with SAC105 spheres, (b) matched paste and spheres,

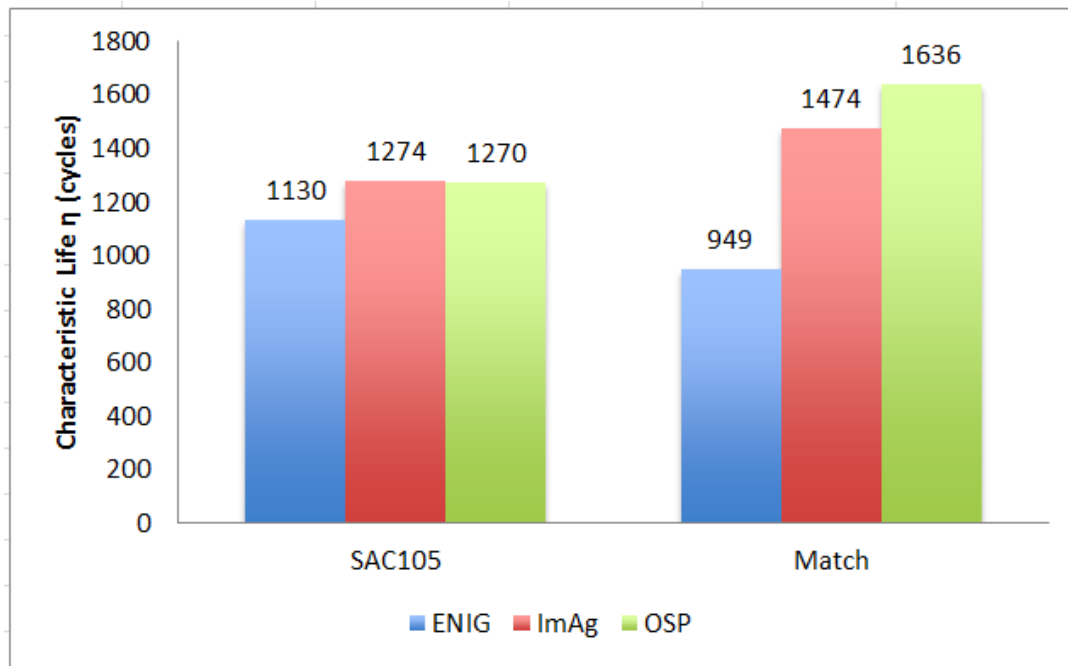
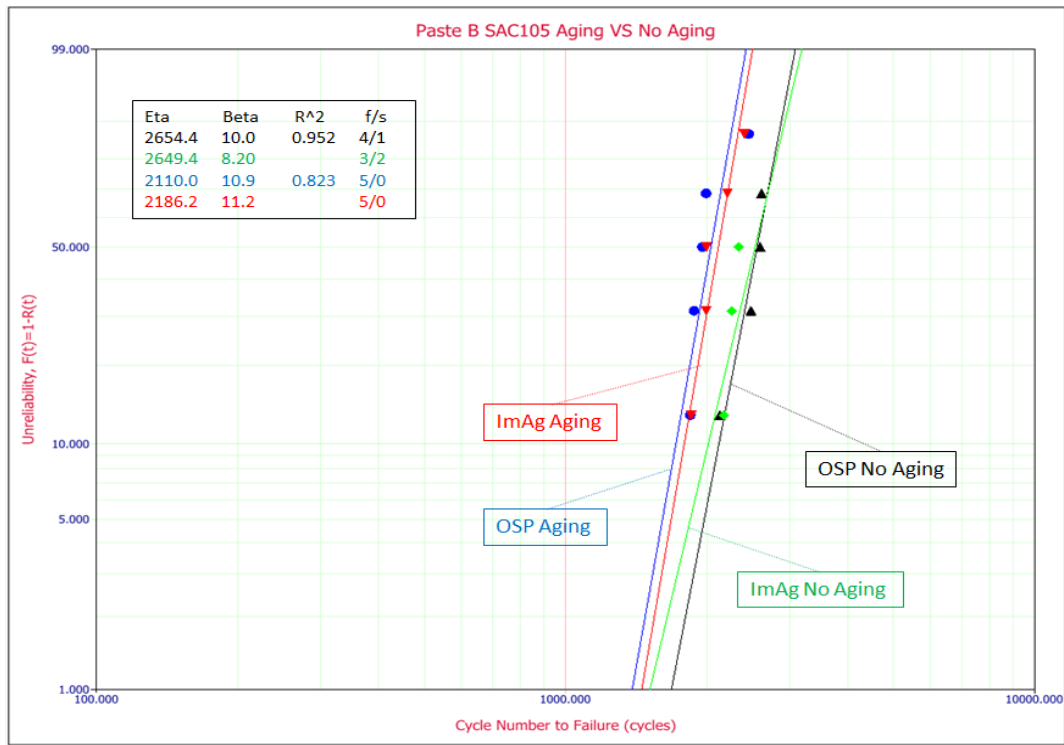


Figure 4.18 Characteristic life values for 15mm BGA with Paste I on each surface finish

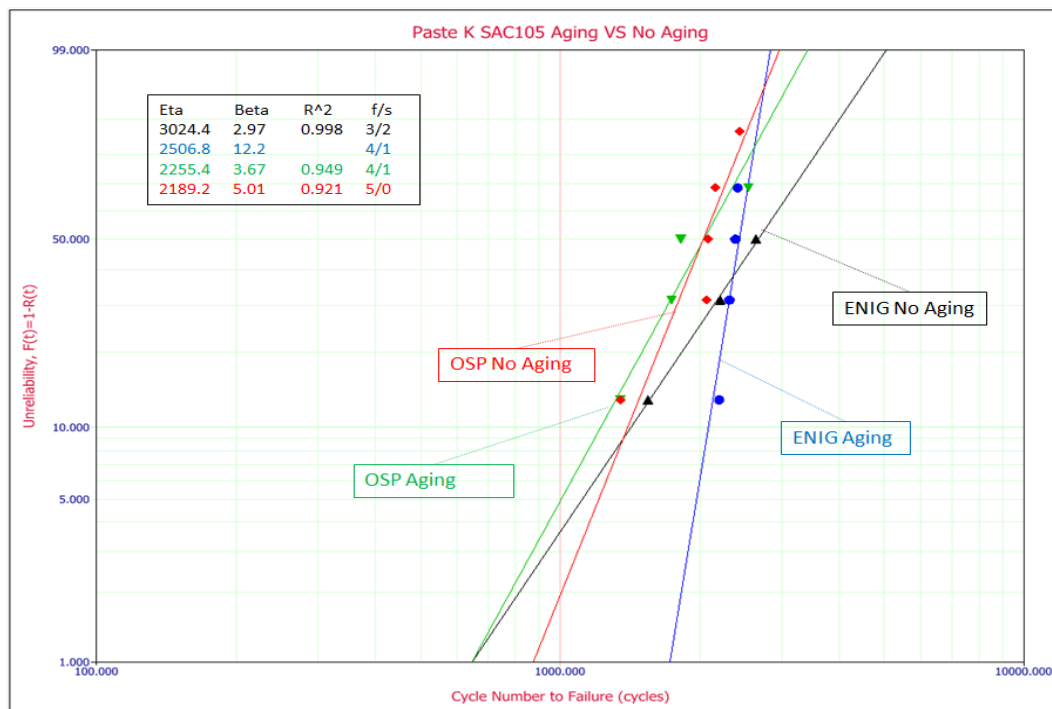
From Figure 4.18, we observe that for Paste I, ENIG is less reliable than OSP and ImAg. So if a BGA sphere is mixed with doped solder paste, it's not always true that ENIG will have the best reliability compared to OSP and ImAg. Sometimes dopants added in SAC solder paste are a more important influence on solder joint reliability than surface finish.

4.2.2.3 Reliability for BGA Package with Aging Effect

The list of Weibull plots below depict reliability degradation of the 15mm BGA packages with different pastes subjected to several of aging preconditioning.



(a)



(b)

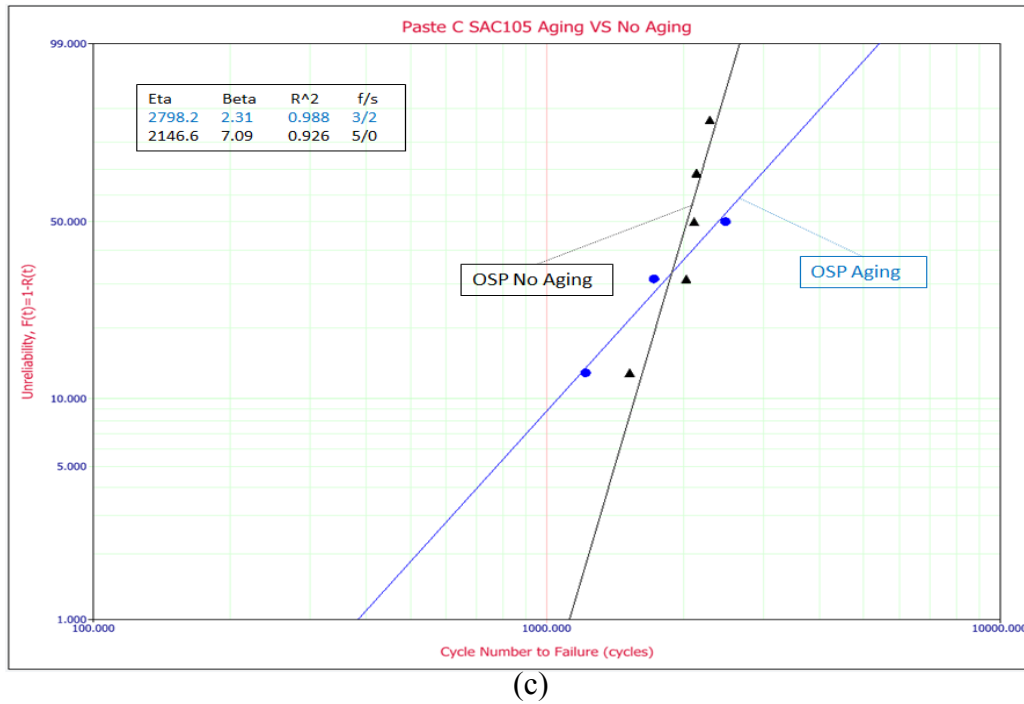


Figure 4.19 Weibull plots for 15mm BGA with different surface finishes considering aging effect

(a) Paste B with SAC105 spheres, (b) Paste B with SAC105 spheres, (c) Paste C with SAC105 spheres

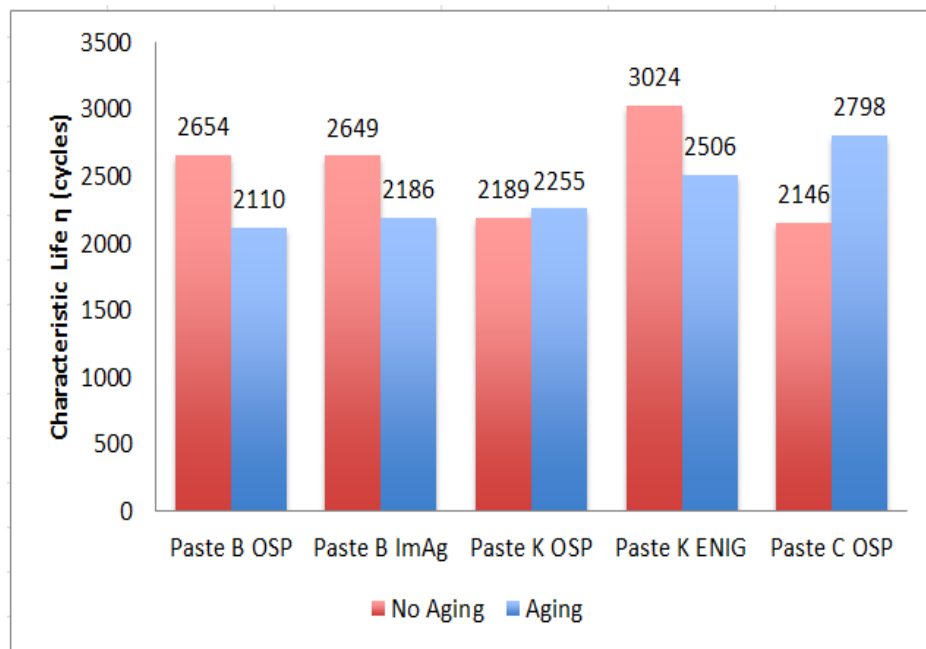


Figure 4.20 Characteristic life values for 15mm BGA considering aging effect

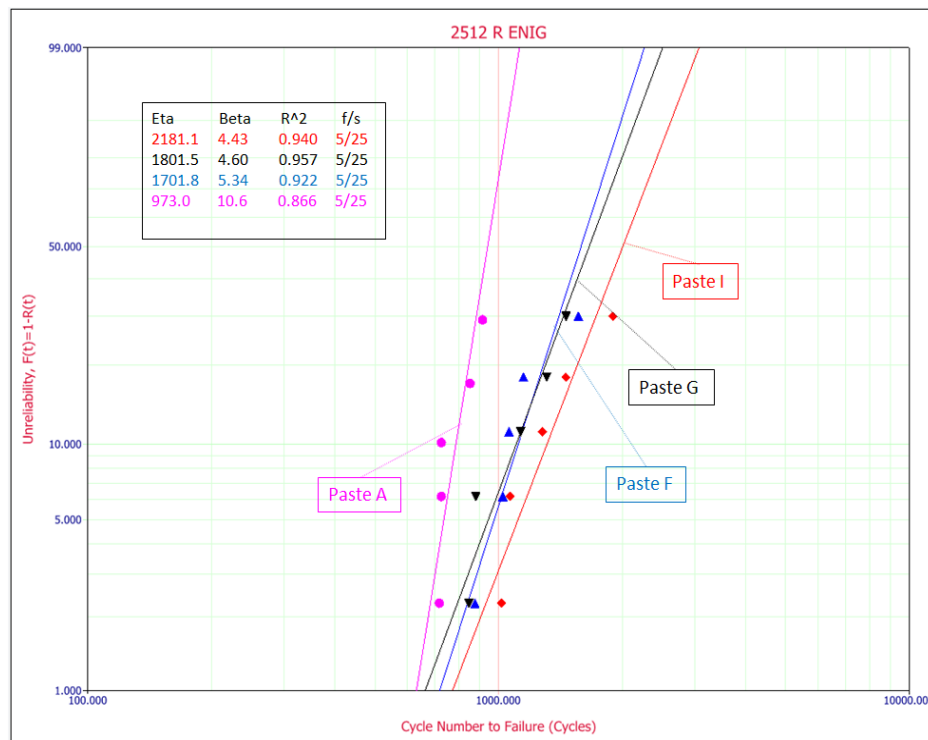
Figure 4.20 summarizes the characteristic life degradation of the 15mm BGA package with SAC105 sphere after aging at 125°C for 12 months. Reliability degradation is observed for Paste B with OSP finish, Paste B with ImAg finish, and Paste K with ENIG finish. The characteristic life for Paste B with OSP finish and SAC105 sphere was reduced from 2654 to 2110 thermal cycles, which is a 20.5% degradation after aging. For Paste B with ImAg finish and SAC105 sphere the characteristic life was reduced from 2649 to 2186 thermal cycles, which is a 17.5% degradation after aging. For Paste K with ENIG finish and SAC105 sphere the characteristic life was reduced from 3024 to 2506 thermal cycles, which is a 17.1% degradation after aging. These results correspond to Cong's study [35] that long-term isothermal aging at elevated temperature can cause degradation of reliability for BGA package.

In Hai's dissertation [93] he investigated the aging effect on reliability of 15mm BGA packages with SAC105 sphere mixed by SAC305 solder paste. From Table 4.1 in his dissertation, he showed that after 12 month aging at 125°C the characteristic life for the 15mm BGA with ImAg finish and SAC105 paste was reduced from 2926 to 1325, which is a 54.7% degradation. If we compare the data with 15mm BGA package with ImAg finish and SAC105 sphere mixed with Paste B, we could see that the doped paste B has an improvement of $(54.7\% - 17.5\%) / 54.7\% = 68\%$ in reliability. Also from Table 5.1, he showed that after 12 month aging at 125°C the characteristic life for the 15mm BGA with ENIG finish and SAC305 paste, the degradation rate was 33.1%. So if we compare the data with the 15mm BGA package with ENIG finish and SAC105 sphere mixed with Paste K, we could see doped paste K has a improvement of $(33.1\% - 17.1\%) / 33.1\% = 48.5\%$ in reliability. So both doped Paste B and Paste K deliver higher reliability than SAC305 paste.

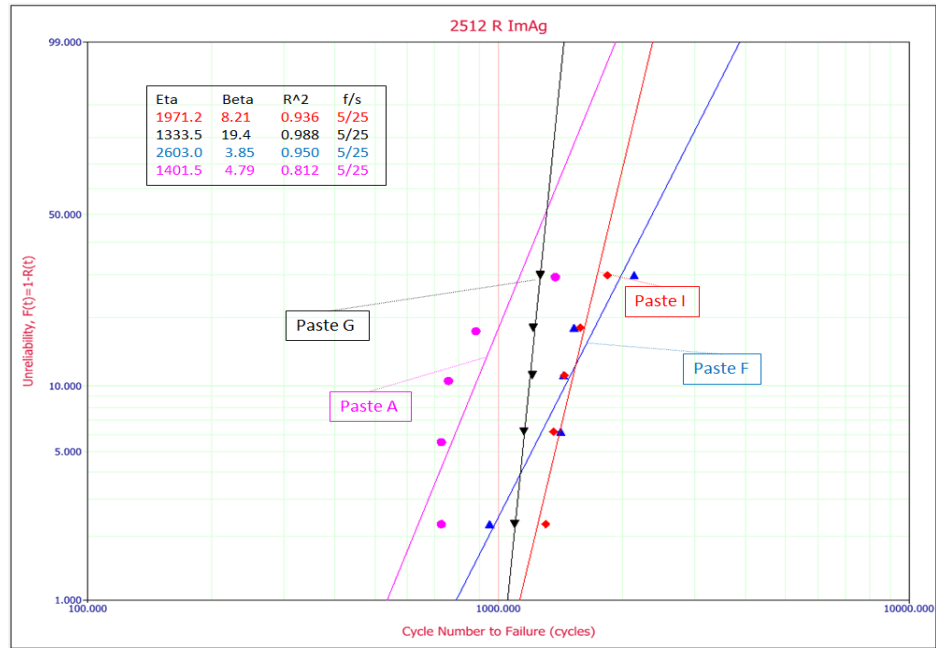
One interesting finding from Figure 4.20 is that for the 15mm BGA package with OSP finish and SAC105 sphere mixed with Paste K and Paste C, after aging the characteristic life values are improved, in other words, aging helps enhance reliability in these cases. For the 15mm BGA package with OSP finish and SAC105 sphere mixed with Paste K and Paste C, reliability is increase by 2.9% and 23.3%, respectively.

4.2.2.4 Reliability for 2512 SMR Package

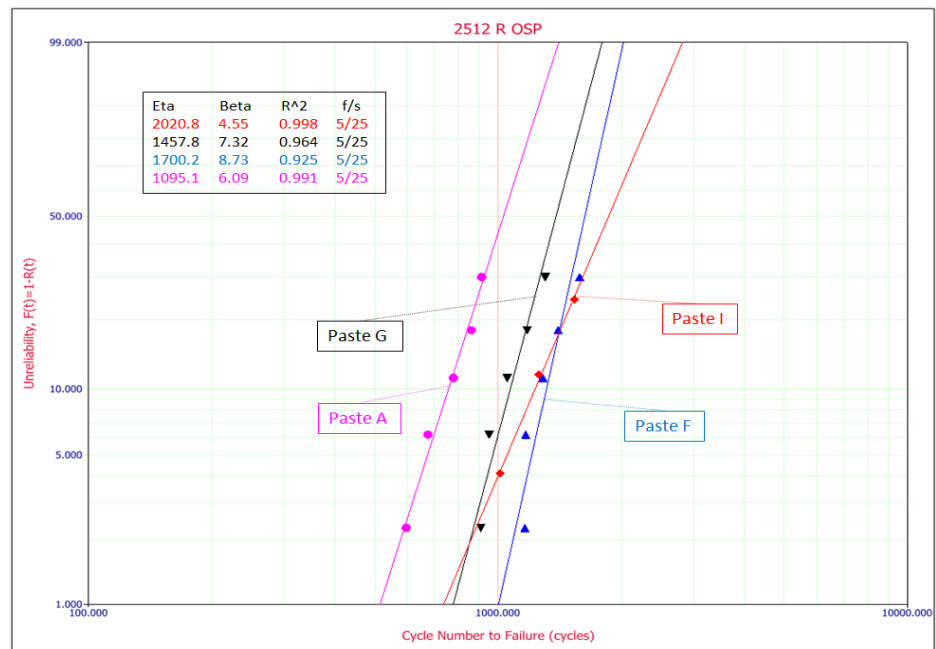
Figure 4.21 shows Weibull data for 2512 SMRs assembled with Paste F, G, I, and A. Figure 4.22 summarizes characteristic life values from the same data set.



(a)

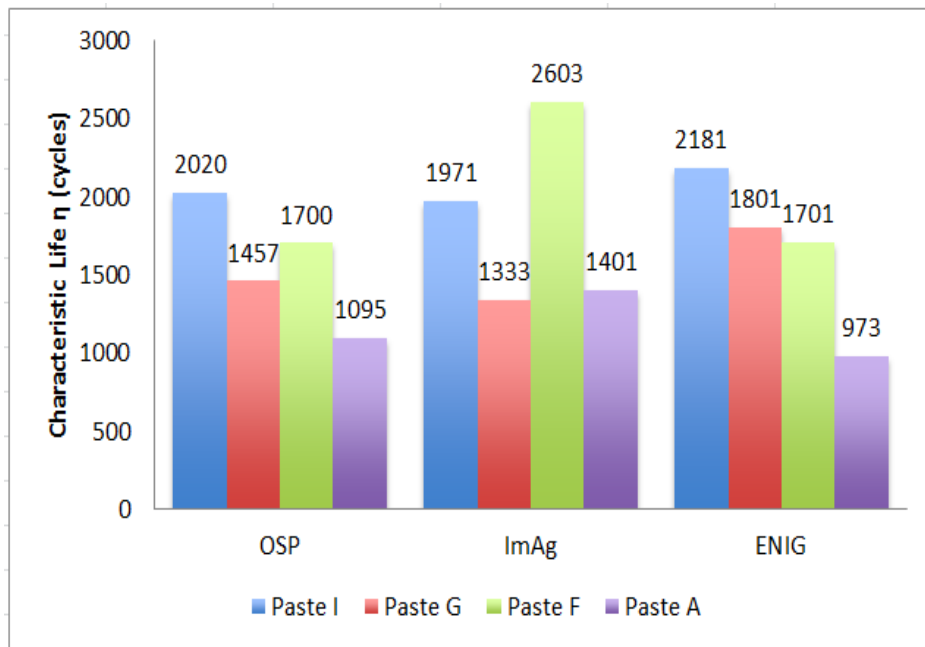


(b)



(c)

Figure 4.21 Weibull plots for 2512 SMR with Paste F, G, L, and A on each surface finish: (a) ENIG, (b) ImAg, (c) OSP.



(a)



(b)

Figure 4.22 Characteristic life values for 2512 SMR with Paste A, F, G, and I: (a) paste comparison, (b) surface finish comparison

From Figure 4.22 (a) we can conclude that for SMR components, Paste A usually has the worst reliability. Paste I and Paste F have better reliability. Paste G performs better than Paste A, but generally worse than Paste I and F. Considering surface finish effect, Figure 4.22 (b) shows that for Paste I and Paste G, ENIG has the best reliability, and ImAg has the worst. While for Paste F and Paste A, ImAg has higher reliability than ENIG. Research by Hai [93] has shown that 2512 SMR sometimes exhibits higher characteristic life values on ImAg surface finish than on ENIG, reversing the reliability trend observed with BGA packages. He observed that crack propagation in the area of the joint under the resistor was more likely to miss-direct into the bulk for ImAg surface finish boards, and more likely to follow the component-side near-IMC region in ENIG and ENEPIG boards. Some results shown in Figure 4.22 (b) and initial cross-section for SMR agrees with his work.

Chapter 5

Failure Analysis

5.1 Introduction

Cracks in solder joints cause increasing electrical resistance and eventual open circuits in BGA components. During thermal aging and cycling, the solder joint undergoes deformation due to the CTE mismatch between the solder joint and the PCB and the component, as well as local CTE differences between grains within the solder. Solder microstructural changes include IMC layer growth at PCB/solder joint/package interface or along grain boundaries in the solder bulk and grain coarsening over time and temperature. The IMC layer is relatively brittle and, over time/temperature, consumes a larger fraction of the solder ball, so cracks are favored to propagate along them and finally cause solder joint failure. Solder recrystallization is also frequently observed in fatigue failures wherein cracks are formed away from the solder interfaces and along the recrystallized grains within the bulk of the solder at positions where the stress is high. Components are prepared into samples and a cross-sectioning method is used to assess failure analysis of solder joints [94-100].

5.2 Typical Microstructure of SAC BGA Solder Joint

For SAC solder systems with ImAg or OSP surface finish, typical IMC layers are Cu_6Sn_5 and Cu_3Sn at the Sn/Cu interface and Ag_3Sn precipitate in the solder bulk [101]. Cu_3Sn exists only at higher copper concentration, therefore is not seen within the bulk of the solder. Initially Cu_6Sn_5 forms adjacent to the copper layer during the reflow process, then during isothermal aging and cycling, Cu_3Sn forms by solid-state diffusion between the copper pad and the Cu_6Sn_5 layer. The morphology of Ag_3Sn precipitate can be particle-like, needle-like, or plate-like depending on different cooling rate during reflow process. Volume fraction of the fine Ag_3Sn IMC particles in

the bulk alloy microstructure of SAC solder alloy increases with higher Ag concentration. Figure 5.1 shows a typical microstructure of SAC solder joint with ImAg or OSP surface finish.

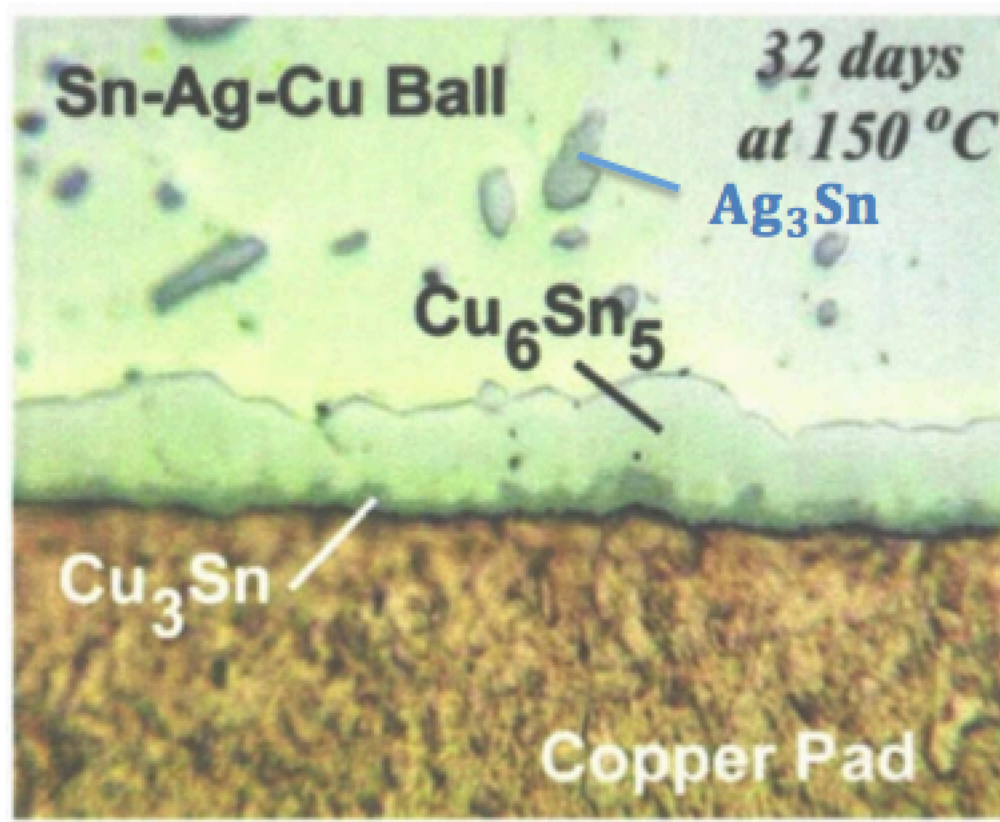


Figure 5.1 Typical microstructure of SAC solder joint with ImAg or OSP finish

For SAC solders with ENIG plating, the IMC layer becomes $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ and $(\text{Ni}, \text{Cu})_3\text{Sn}_4$ [102]. After reflow, the IMC are irregular and grow in a needle-like manner and the composition of the IMC is a $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ ternary compound. During thermal aging, a small number $(\text{Ni}, \text{Cu})_3\text{Sn}_4$ IMC started forming between the $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ IMC and the copper pad with Ni coated on top. After further aging the morphology of IMC layer changed from scallop to planar-like and finally layer-like, with less surface roughness. The presence of the Ni layer in ENIG/ENEPIG acts as a diffusion barrier, which retards Cu dissolution into the solder to insure better reliability. Figure 5.2 shows the board-side IMC region for the case of SAC305 on ENIG.

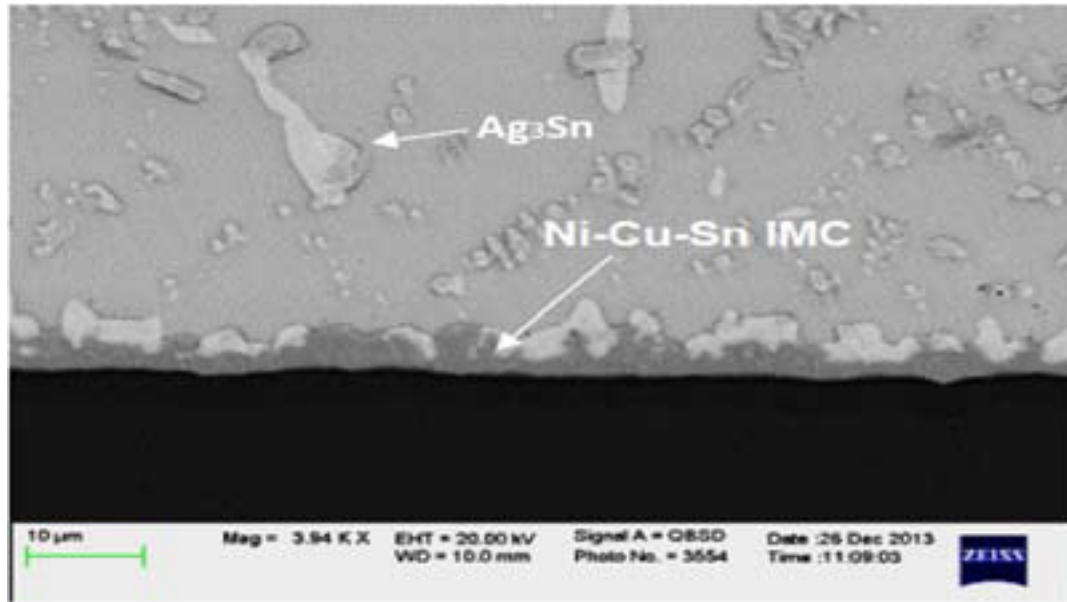


Figure 5.2 Typical microstructure of SAC solder joint with ImAg or OSP finish

In addition to scanning electron microscopy, we also use optical microscopy, such as polarized light microscopy (PLM) to examine the grain orientations change of the solder bulk during thermal aging and cycling. The PLM we used for this project is an Axio Imager for polarized light microscope made by Carl Zeiss.

5.3 Microstructure of 15mm BGA Solder Joint with Paste B

Paste B is a Bi-doped SAC based alloy with six elements, the composition of which is 90.9Sn-3.8Ag-0.7Cu-3.0Bi-1.4Sb-0.15Ni. This doped solder paste is better known in the automotive industry by the name of Innolot. It is designed for use in demanding environments (high temperature and vibration) that are beyond the reliability performance capabilities of standard SAC alloys. From previous data analysis section, we found that Paste B experienced much lower degradation in material properties as a function of aging time, and thus had an improvement in the reliability. Figure 5.3 shows a SEM image for a representative microstructure for a 15mm BGA package mixed with Paste B.

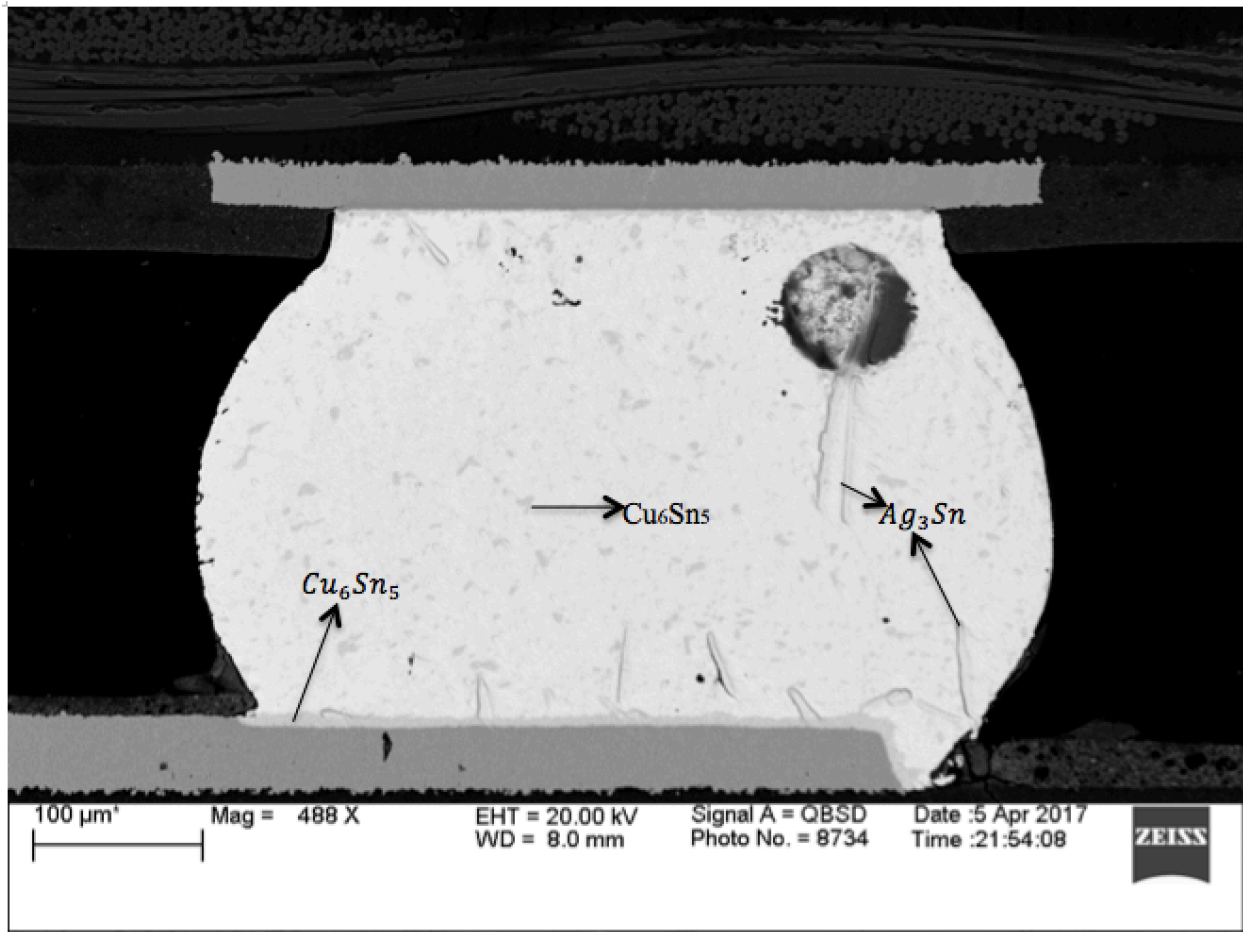


Figure 5.3 Representative SEM image for microstructure of 15mm BGA package with Paste B and OSP finish

Figure 5.3 illustrates the plate-like Ag_3Sn IMC and particle-like Cu_6Sn_5 IMC inside the solder bulk, together with Cu_6Sn_5 IMC layer in the package side. Figure 5.4 shows a magnified image of the microstructure of a 15mm BGA Package with Paste B and OSP surface finish.

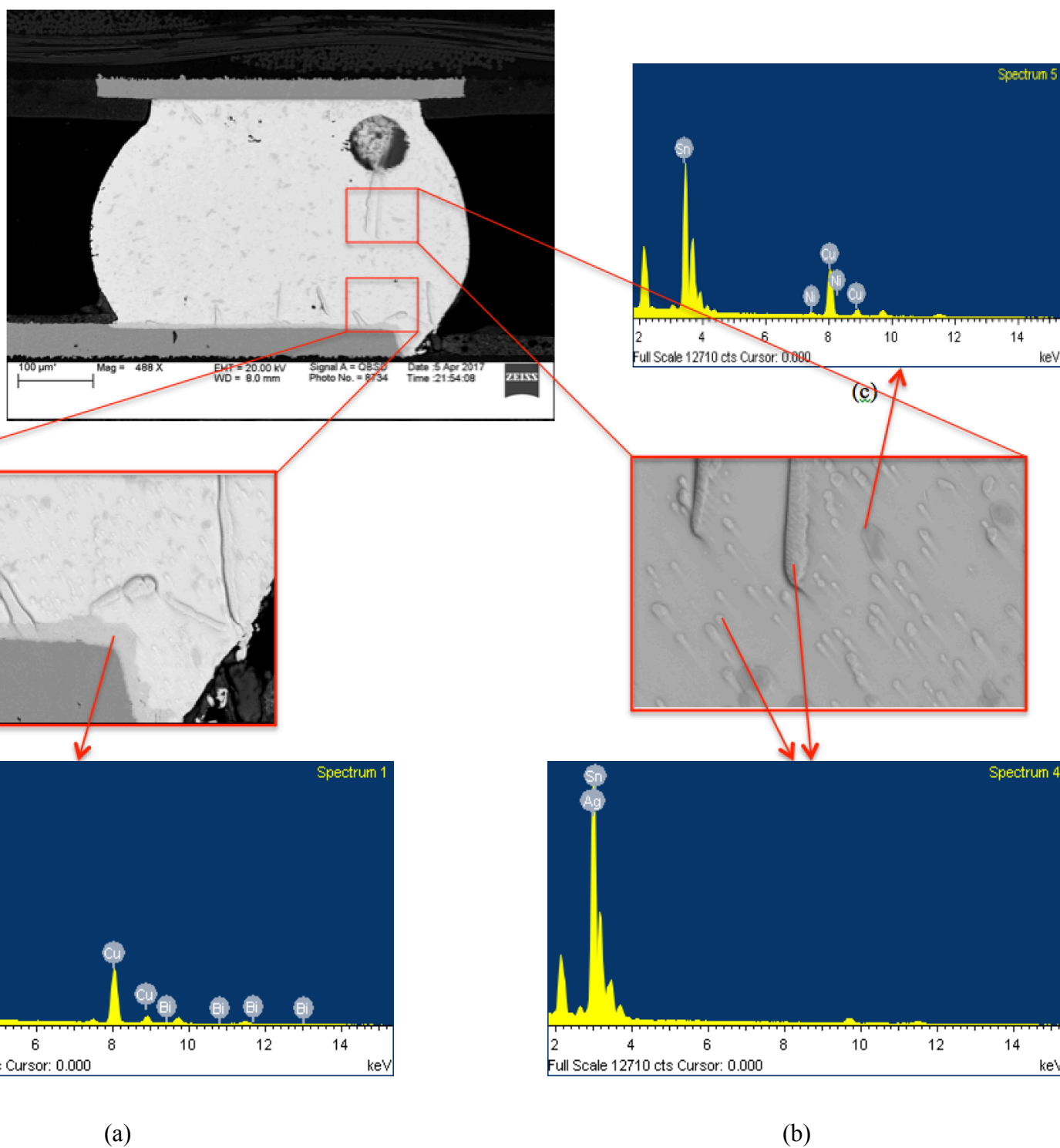
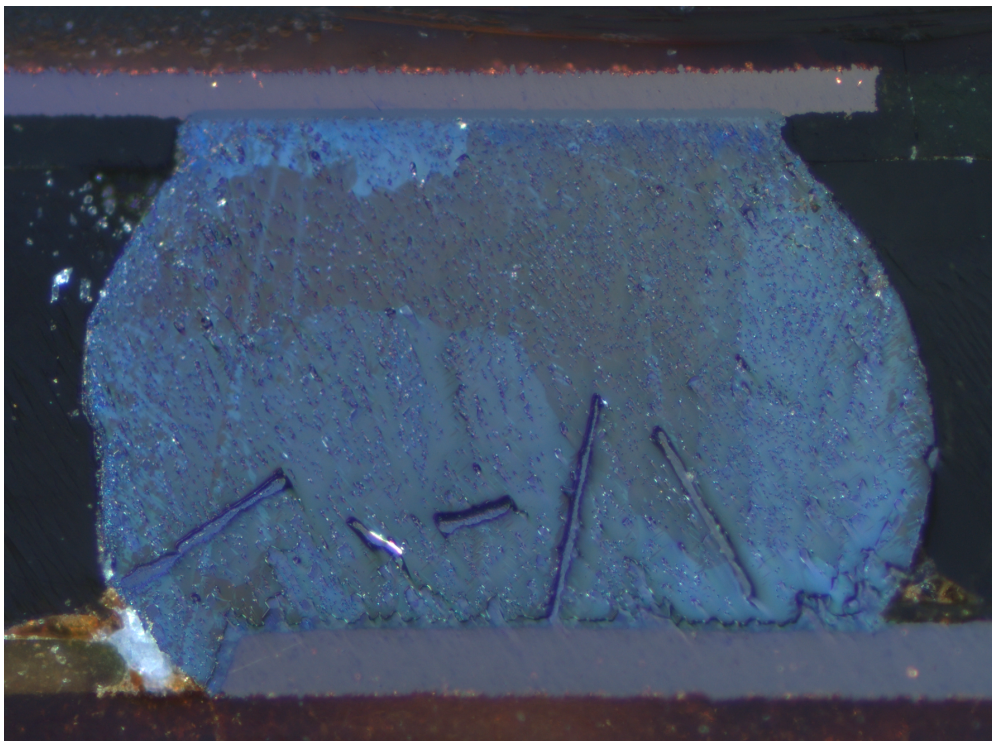


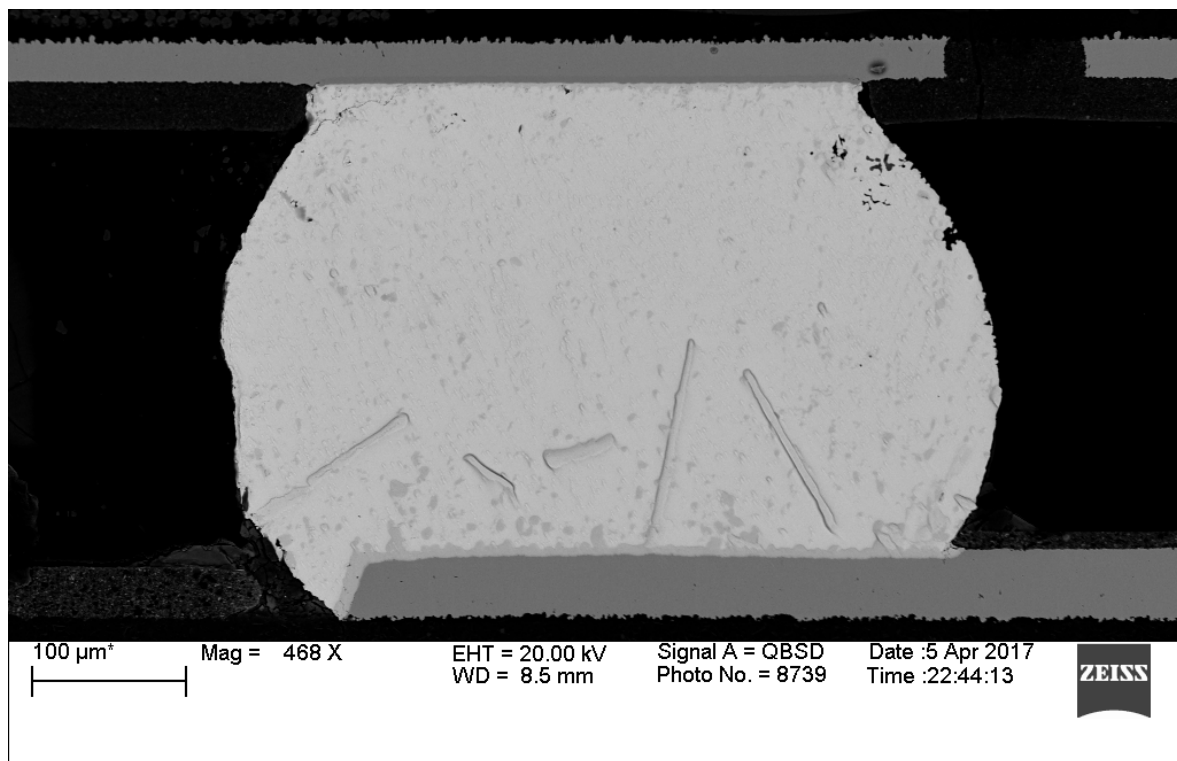
Figure 5.4 Higher magnification SEM and EDX of microstructure for 15mm BGA package with Paste B: (a) IMC layer, (b) plate-like and particle-like Ag_3Sn bulk IMC, (c) particle-like Cu_6Sn_5 bulk IMC

From Figure 5.4 we notice that the component-side IMC layer is actually $(\text{Cu, Bi})_6\text{Sn}_5$, instead of Cu_6Sn_5 . Additional bismuth may enhance the stability as well as limit the thickness of the IMC layer, and lead to better reliability for the solder joint. IMC layer thickness analysis will be discussed below. For bulk IMC, there are particle-like $(\text{Cu, Ni})_6\text{Sn}_5$ IMC distributed evenly across the solder joint, where nickel comes from the solder paste dopant. Besides plate-like shape, there are also particle-like Ag_3Sn bulk IMC, the size of which is much smaller than $(\text{Cu, Ni})_6\text{Sn}_5$ bulk IMC and distributes evenly across the whole solder joint.

Figure 5.5 shows a polarized light microscope image and corresponding SEM image for a 15mm BGA package solder joint with Paste B. Again we can easily find large plate-like Ag_3Sn bulk IMC. The figure also illustrates the recrystallization phenomenon in the solder bulk, where different grain orientations and grain boundaries are generated.



(a)

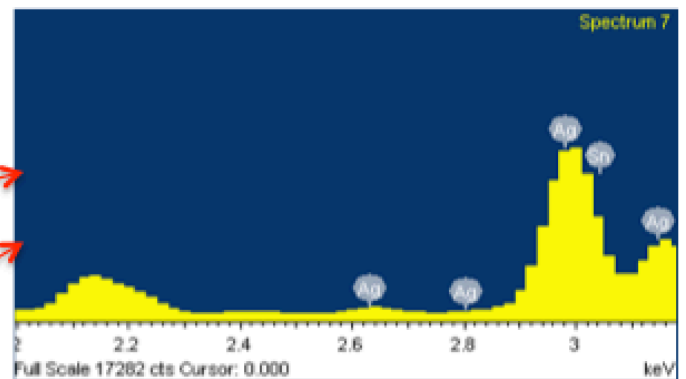
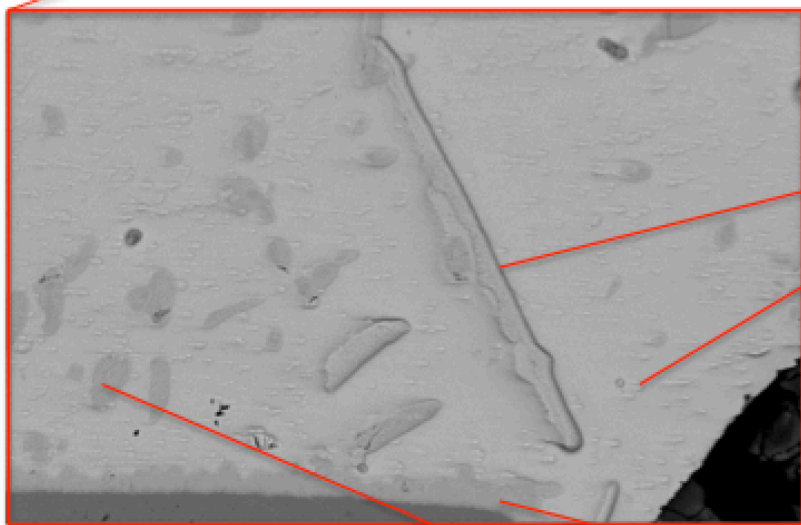
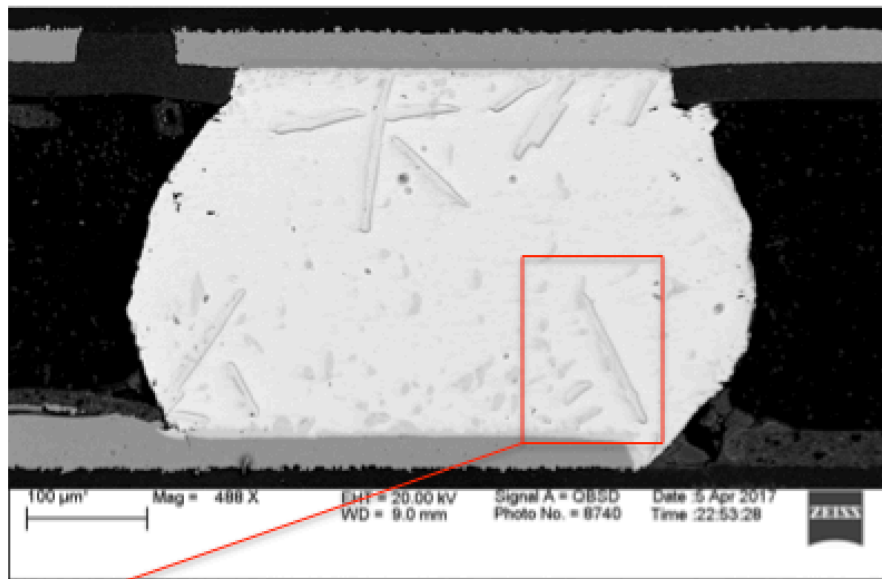


(b)

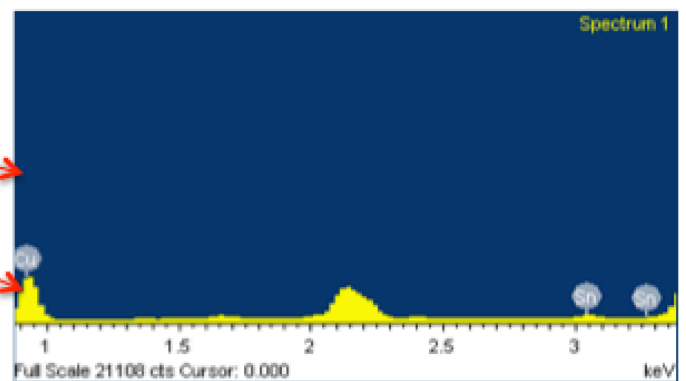
Figure 5.5 Microstructure for 15mm BGA package solder joint with Paste B: (a) polarized light microscope image, (b) SEM image.

5.4 Microstructure of 15mm BGA Solder Joint with Paste F

Similar to Paste B, Paste F is also a Bi-doped SAC based alloy but with four elements, the composition of which is 92.77Sn-3.41Ag-0.52Cu-3.3Bi. Paste F also contains high silver and bismuth content, but no antimony and nickel. Figure 5.4 shows a SEM and EDX image for the microstructure of a 15mm BGA Package with Paste F and ImAg surface finish.



(a)



(b)

Figure 5.6 SEM and EDX of microstructure for a 15mm BGA package with Paste F and ImAg finish: (a) plate-like and particle-like Ag_3Sn bulk IMC, (b) Cu_6Sn_5 bulk IMC and IMC layer

It can be found in Figure 5.6 that the component-side IMC layer is actually Cu_6Sn_5 , unlike Paste B who also contains bismuth in the IMC layer. For the bulk IMC, there are particle-like Cu_6Sn_5 IMC distributed across the solder joint, as well as plate-like and particle-like Ag_3Sn bulk IMC. Again the size of particle-like Ag_3Sn is much smaller than Cu_6Sn_5 bulk IMC.

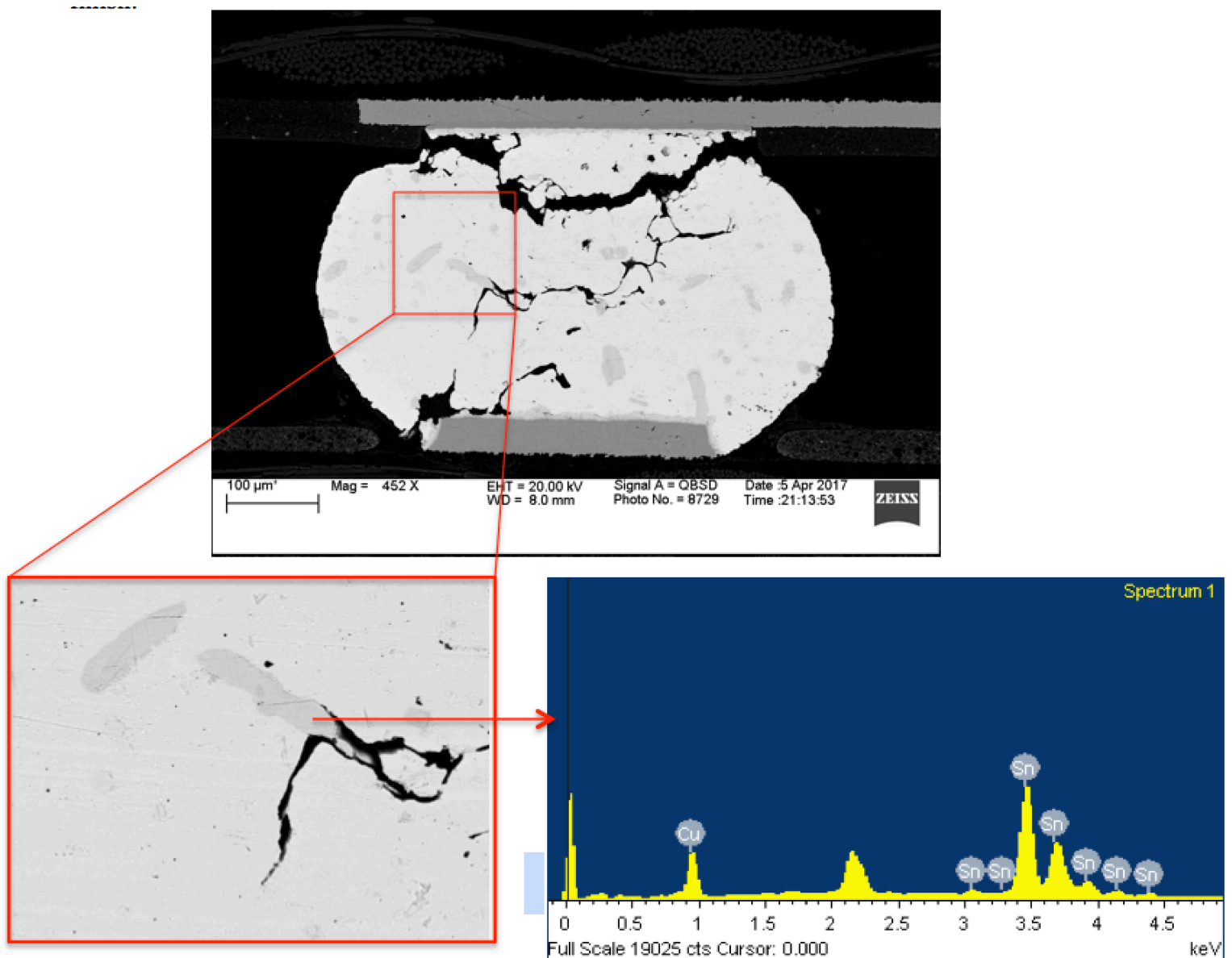
Figure 5.7 shows a polarized light microscope image for a 15mm BGA package solder joint with Paste F. Many large plate-like Ag_3Sn bulk IMC can be found. Recrystallization phenomenon in the solder bulk is clear, forming a so-called “beach ball” structure, where different brightness regions in this figure indicate different dominant crystal orientations.



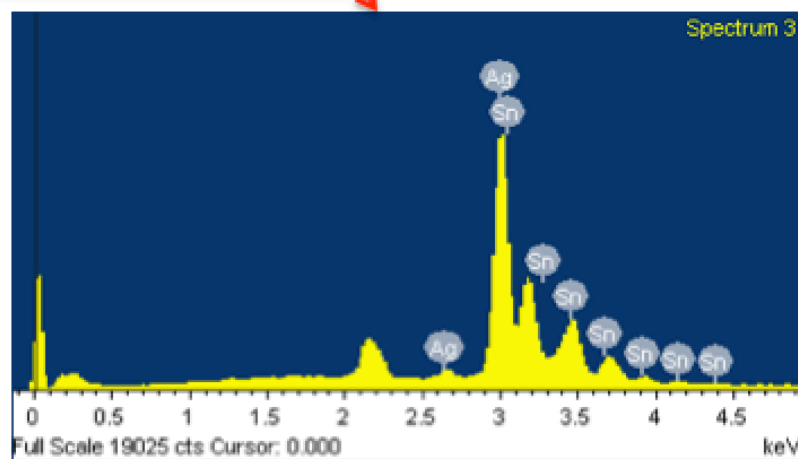
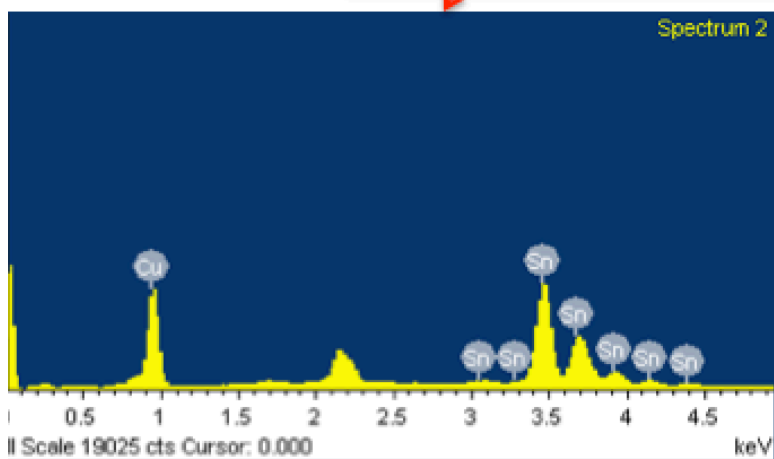
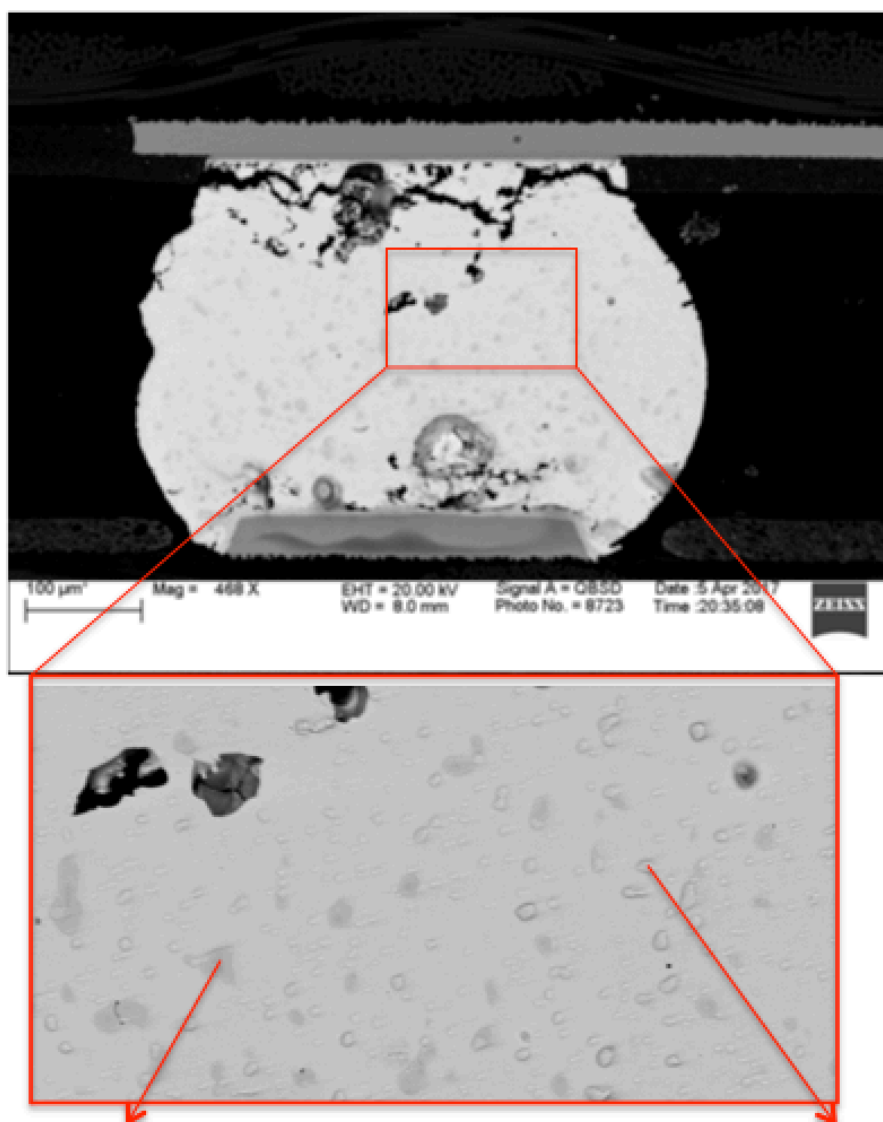
Figure 5.7 Polarized light microscope image of microstructure for a 15mm BGA package solder joint with Paste F including “Beach Ball” structure

5.5 Microstructure of 15mm BGA Solder Joint with Paste A

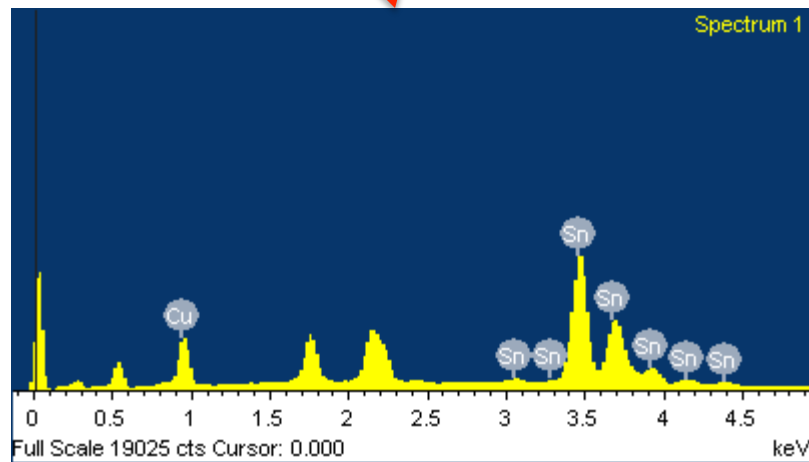
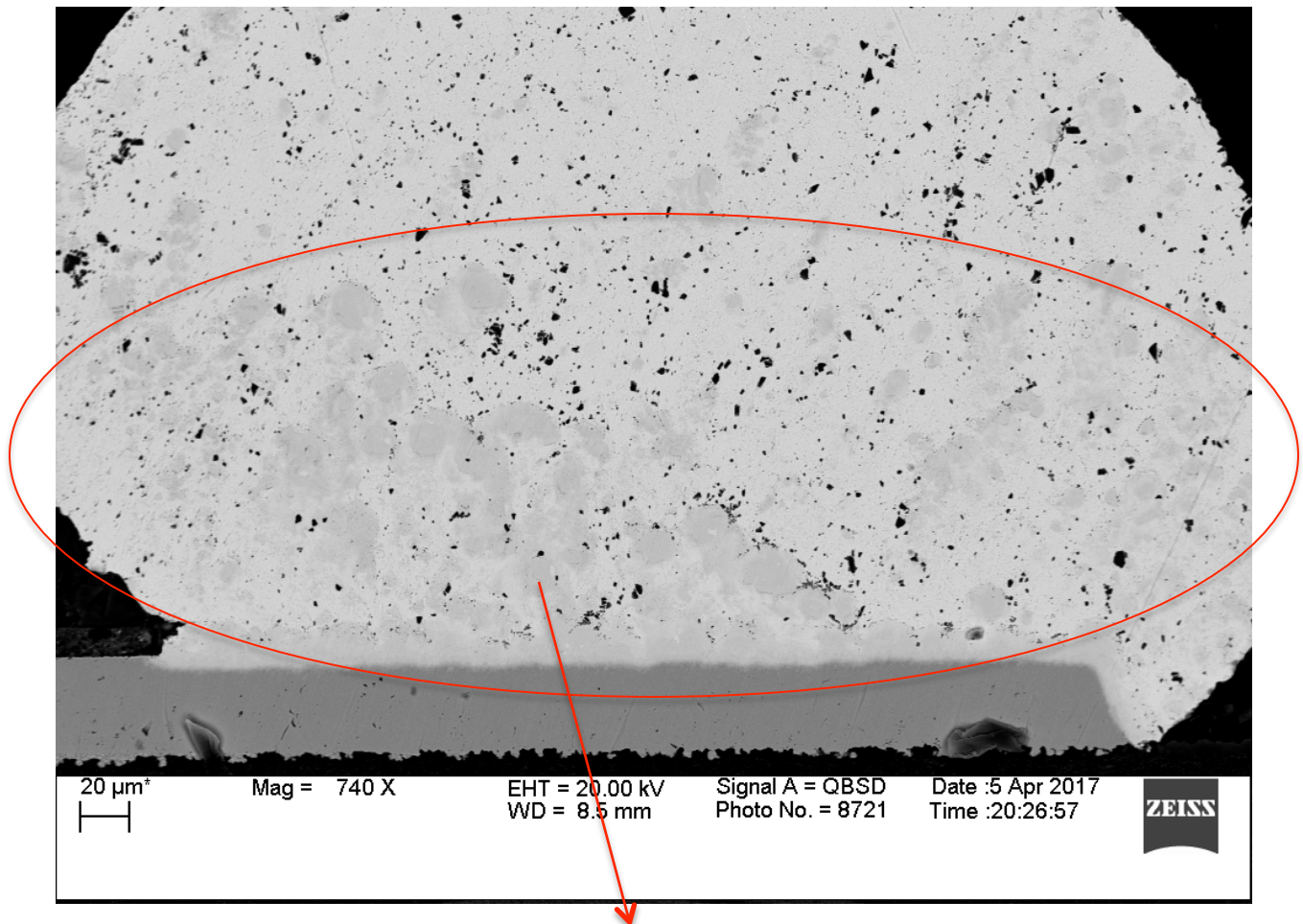
Different from Paste B and F, Paste A contains no bismuth, and it's a SAC based alloy with four elements, the composition of which is 98.47Sn-0.5Ag-1.0Cu-0.03Mn. Compared to Paste B and Paste F, Paste A also has a very low silver content, even lower than traditional SAC105 paste. Due to these two reasons Paste A delivers very low reliability than other pastes. Figure 5.8 shows a SEM and EDX image for microstructure of 15mm BGA Package with Paste A and OSP surface finish.



(a)



(b)

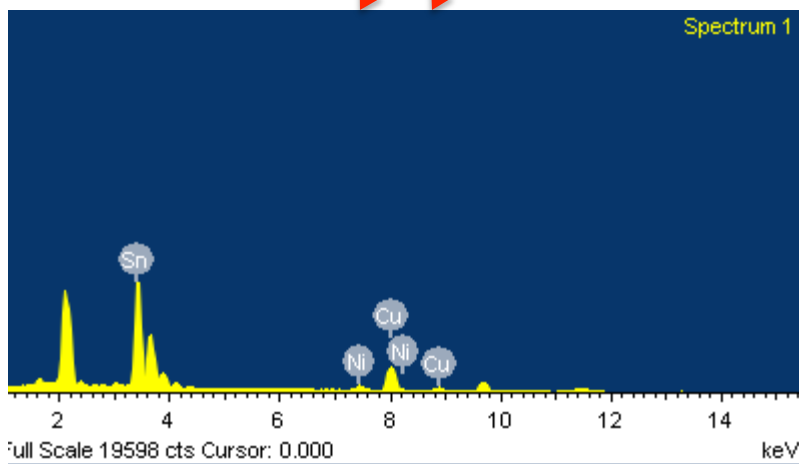
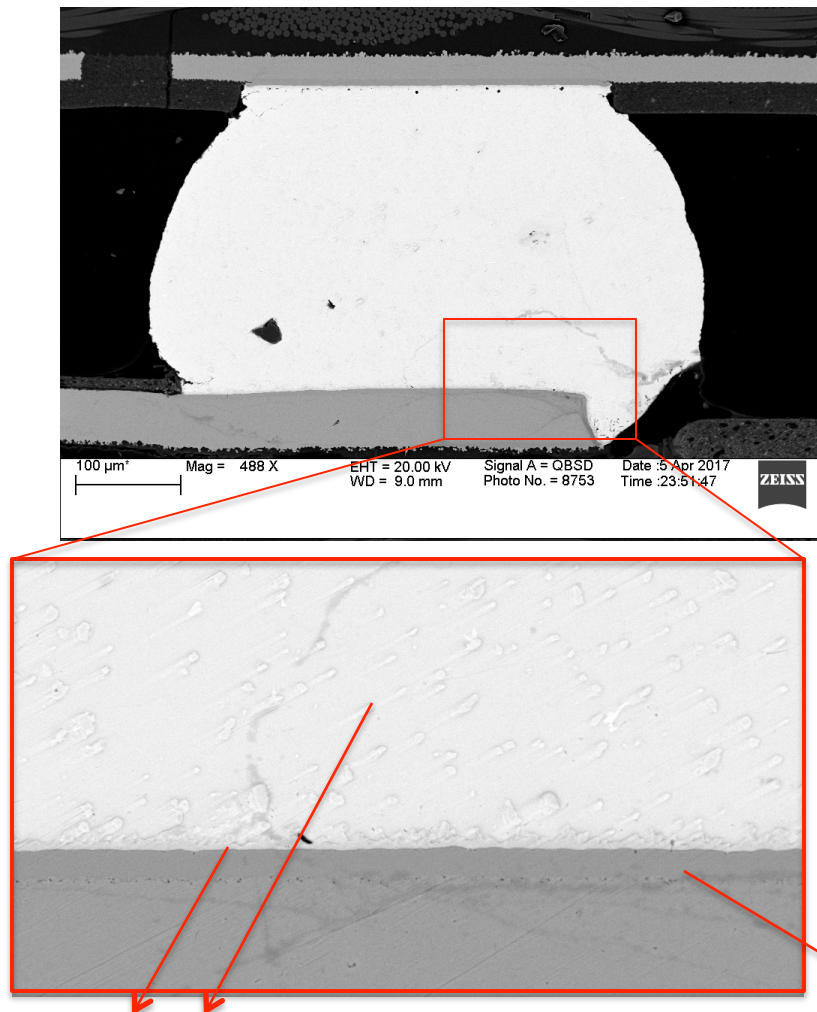


(c)

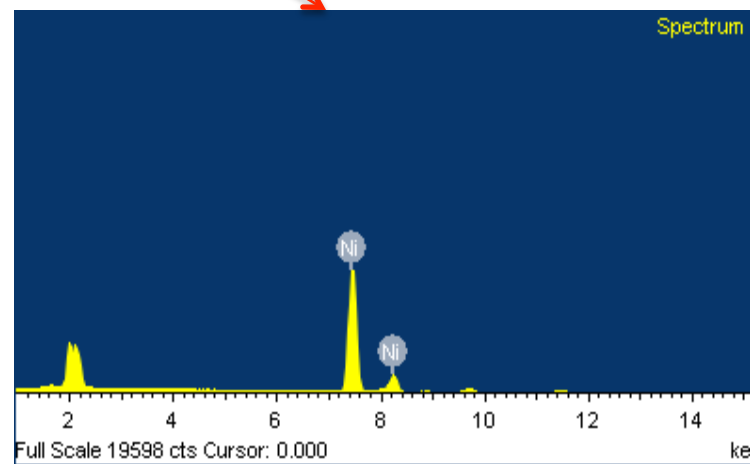
Figure 5.8 SEM and EDX of microstructure for 15mm BGA package with Paste A and OSP finish: (a) matched sphere with plate-like Cu_6Sn_5 bulk IMC, (b) SAC305 sphere with particle-like Ag_3Sn and Cu_6Sn_5 bulk IMC, (c) SAC105 with particle-like Cu_6Sn_5 bulk IMC

Figure 5.8 (a) shows that for a 15mm BGA Package with Paste A and matched solder sphere, plate-like Cu_6Sn_5 can be found inside the bulk, different from Paste B and F where one could only find plate-like Ag_3Sn and particle-like Cu_6Sn_5 bulk IMC. For a 15mm BGA Package with Paste A and SAC305 solder sphere listed in Figure 5.8 (b), both Ag_3Sn and Cu_6Sn_5 bulk IMC are in particle-like shape, with no plate-like IMC. In Figure 5.8 (c) for a 15mm BGA Package with Paste A and SAC105 solder sphere, it shows many particle-like Cu_6Sn_5 IMC cumulated near the solder joint/PCB interfacial area, where the size of each particle is much larger than that with SAC305 solder sphere. These findings may help explain why for Paste A, matched sphere is the most reliable, followed by SAC105 sphere and finally SAC305 sphere.

Figure 5.9 shows a SEM and EDX image for the microstructure of a 15mm BGA Package with Paste A and ENIG surface finish. ENIG finish has an additional nickel layer between the solder joint and PCB copper pad, which acts as a diffusion barrier preventing copper dissolution into the solder to insure better reliability. As we mentioned in section 5.2, for SAC solders with ENIG plating, the IMC layer becomes $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ and $(\text{Ni}, \text{Cu})_3\text{Sn}_4$. Results can be seen in Figure 5.9, which shows a thin layer of $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ IMC, as well as less tiny $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ bulk IMC in the solder joint because of less copper diffusion.



(a)

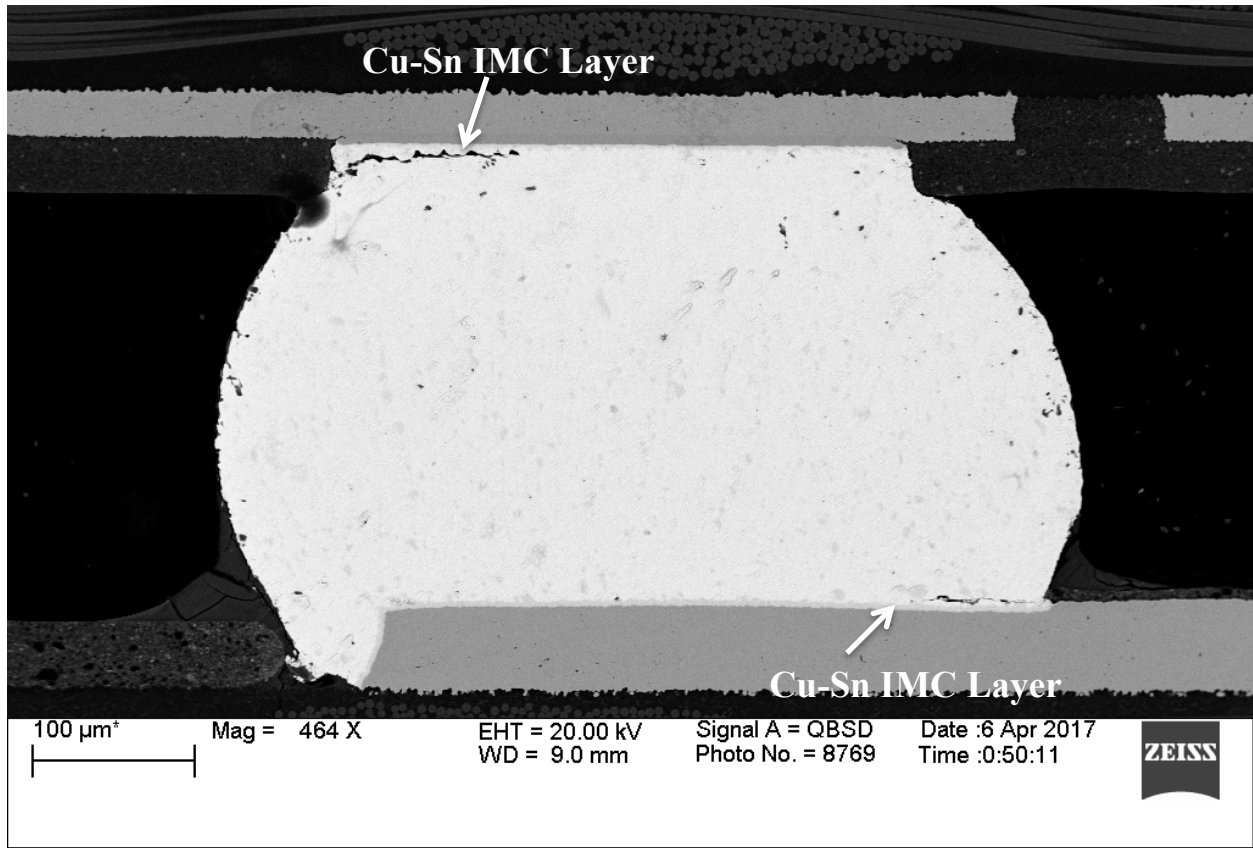


(b)

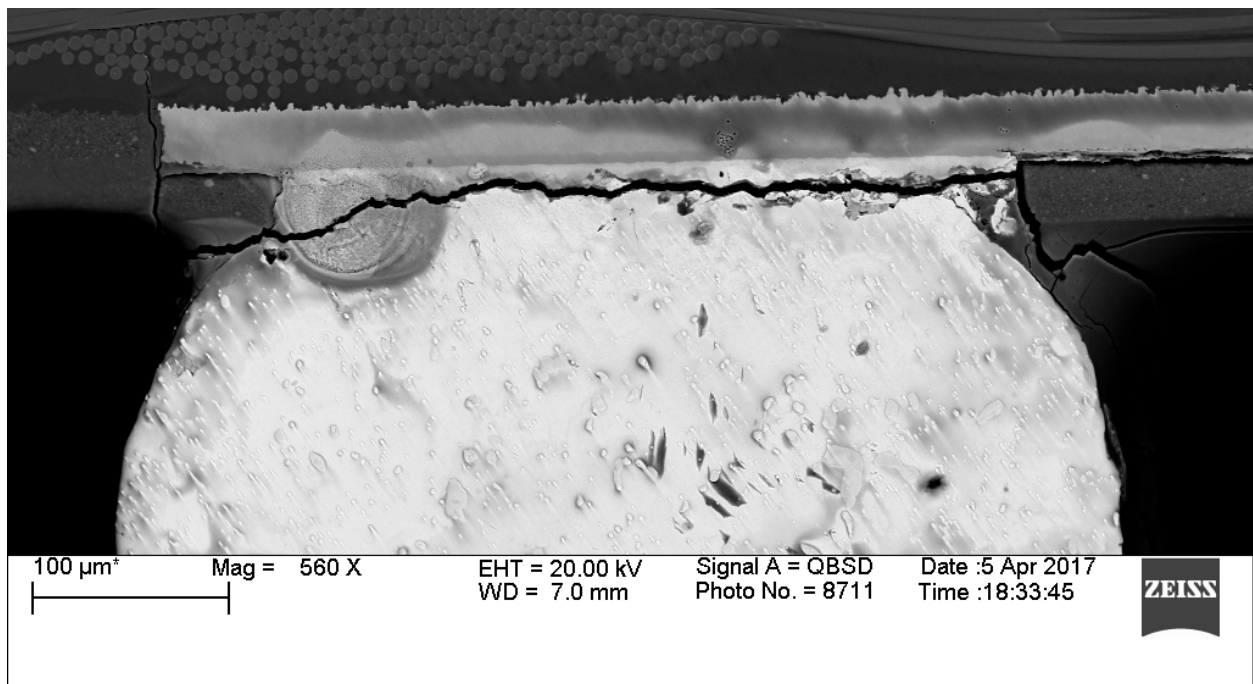
Figure 5.9 SEM and EDX of microstructure for 15mm BGA package with Paste A and ENIG finish: (a) particle-like $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ bulk IMC and IMC layer, (b) nickel layer for ENIG finish

5.6 Crack Propagation and Failure Modes

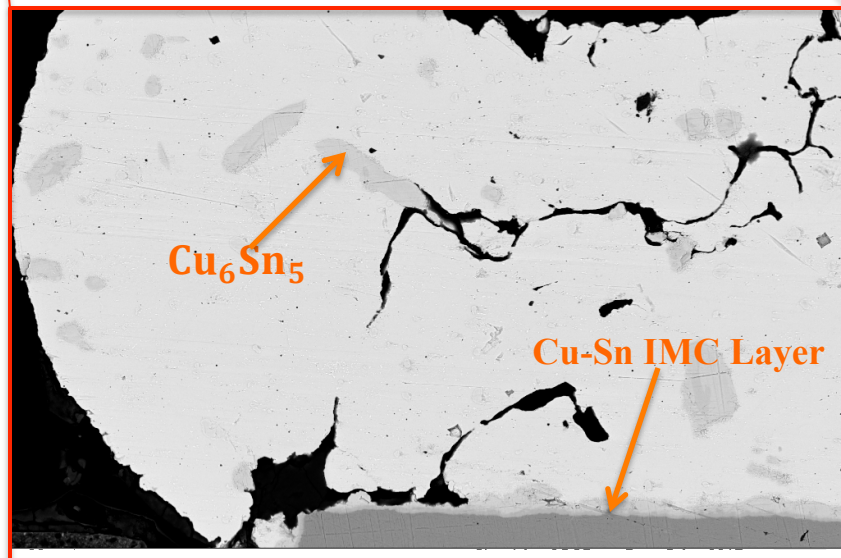
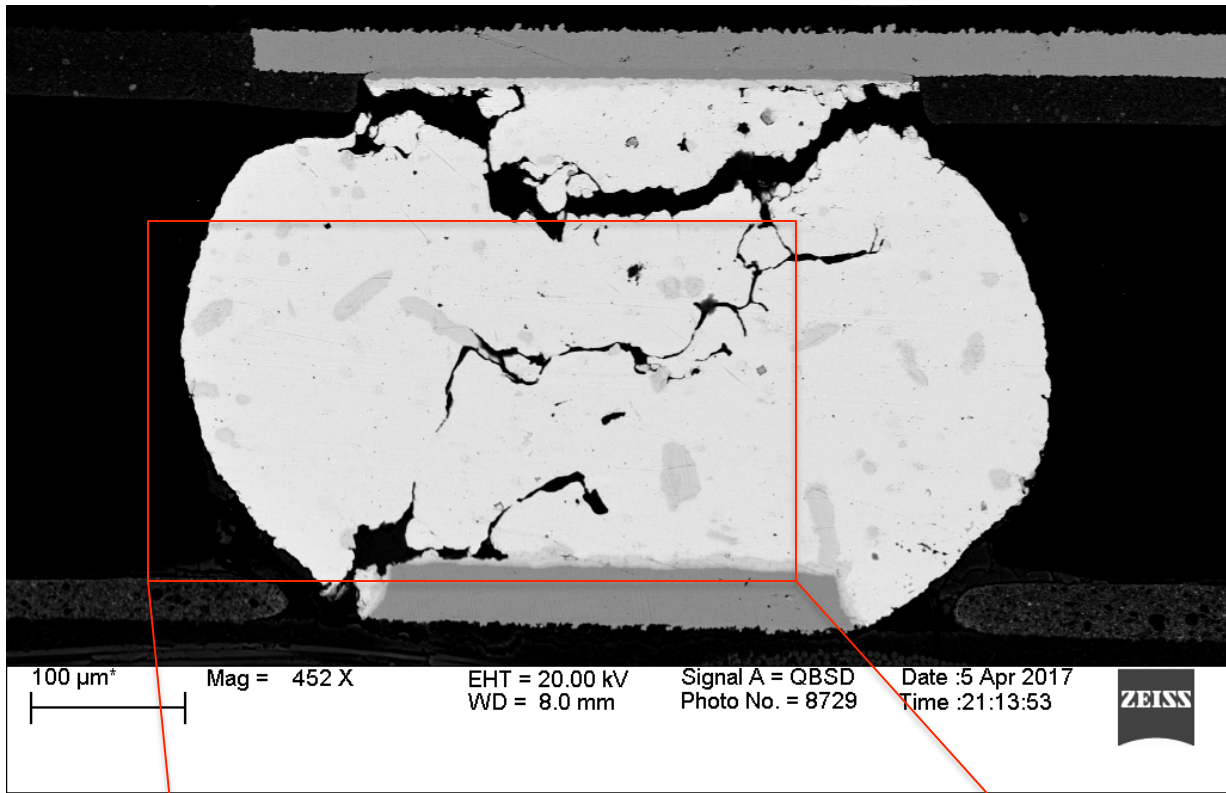
Cracks in solder joints cause increasing electrical resistance and eventual open circuits in BGA components. Cracks usually initiate from the regions with the largest stresses (corner areas for BGA package), and then propagate following stress distribution. During thermal aging and cycling, the solder joint undergoes deformation due to the CTE mismatch between the solder joint and the PCB and the component, as well as local CTE differences between grains within the solder. Solder microstructural changes include IMC layer growth at PCB/solder joint/package interface or along grain boundaries in the solder bulk and grain coarsening over time and temperature. During thermal aging and cycling, the IMC layer in both the component- and board-side interfaces thicken continuously, consuming material from the copper pads and solder joint. The near-interfacial region is often the principal area in which crack initiation and propagation are observed due to high stress concentration and fatigue. Solder recrystallization is also frequently observed in fatigue failures where cracks are formed away from the solder interfaces and along the recrystallized grain boundaries within the bulk of the solder at positions where the stress is high. Typical failure modes for BGA packages are shown in Figure 5.10.



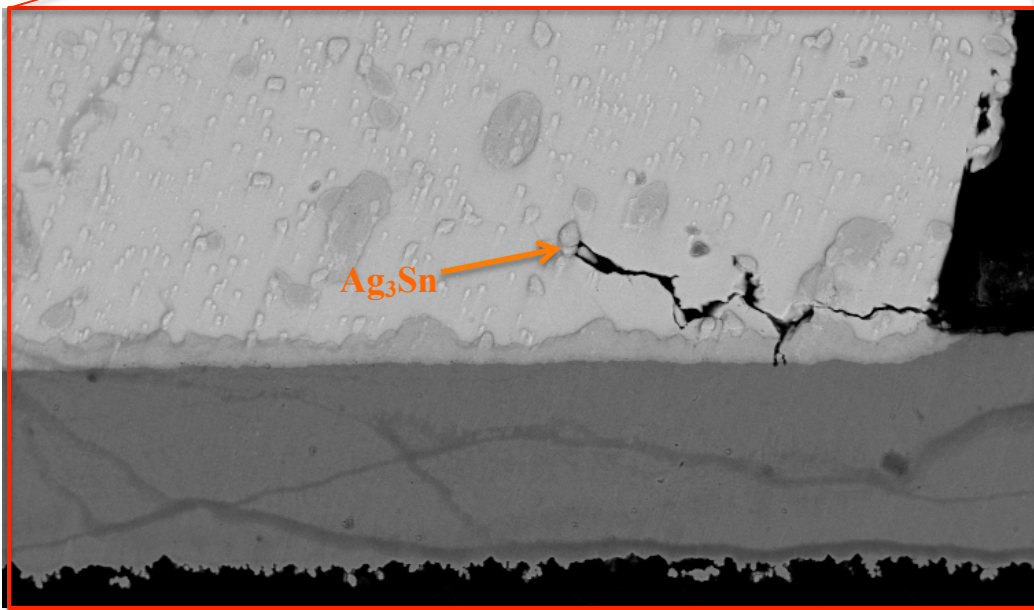
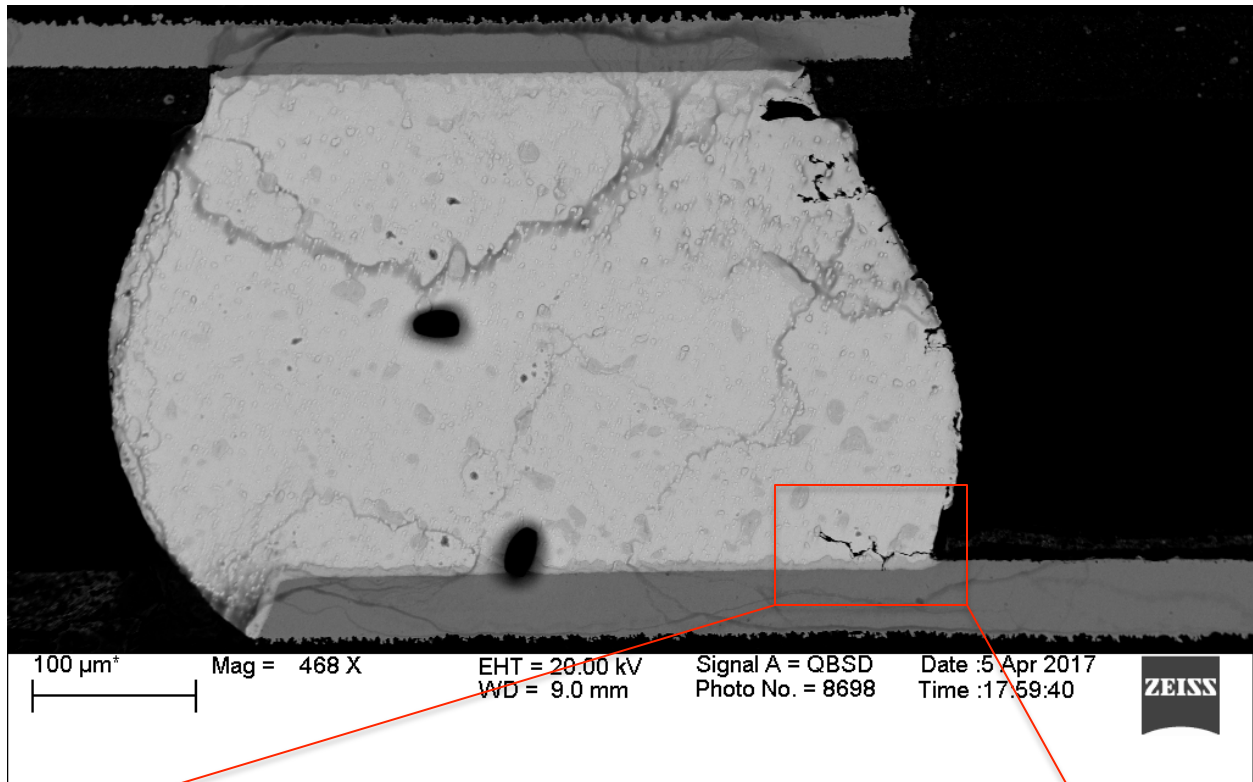
(a)



(b)



(c)



(d)

Figure 5.10 Typical failure modes for BGA package. Crack propagation close to the (a)(b) board-side and package-side IMC layer. (c)(d) Crack propagation through the solder bulk.

Figure 5.10 (a) shows crack propagation along both the board and package side near-interfacial IMC layer region for a 15mm BGA package with Paste C, ImAg finish and SAC105 sphere after 12 months aging at 125°C. Figure 5.10 (b) shows a complete through crack along the package side near-interfacial IMC layer region for a 15mm BGA package with Paste I, OSP finish and SAC105 sphere. Figure 5.10 (c) shows cracks which form initially at the package side corner of solder joint, and extend into the solder bulk with a high angle, for a 15mm BGA package with Paste A, OSP finish and match sphere. Figure 5.10 (c) shows the crack inside the solder bulk goes around the Cu_6Sn_5 bulk IMC. Figure 5.10 (d) shows that cracks initiates at the board side corner of solder joint, propagate along the board side IMC layer, and then go into the solder bulk, and are finally blocked by a Ag_3Sn bulk IMC particle, for a 15mm BGA package with Paste I, OSP finish and SAC305 sphere. Ag_3Sn bulk IMC can sometimes block the propagation of crack through solder bump, thus pastes with high silver content tends to have higher reliability.

A polarized light microscope image can usually show more details about the crack propagation process for failure mode where crack formed away from the solder interfaces and along the recrystallized grain boundaries within the bulk. Figure 5.11 shows a polarized light microscope image together with the corresponding SEM image for a 15mm BGA solder joint with cracks.

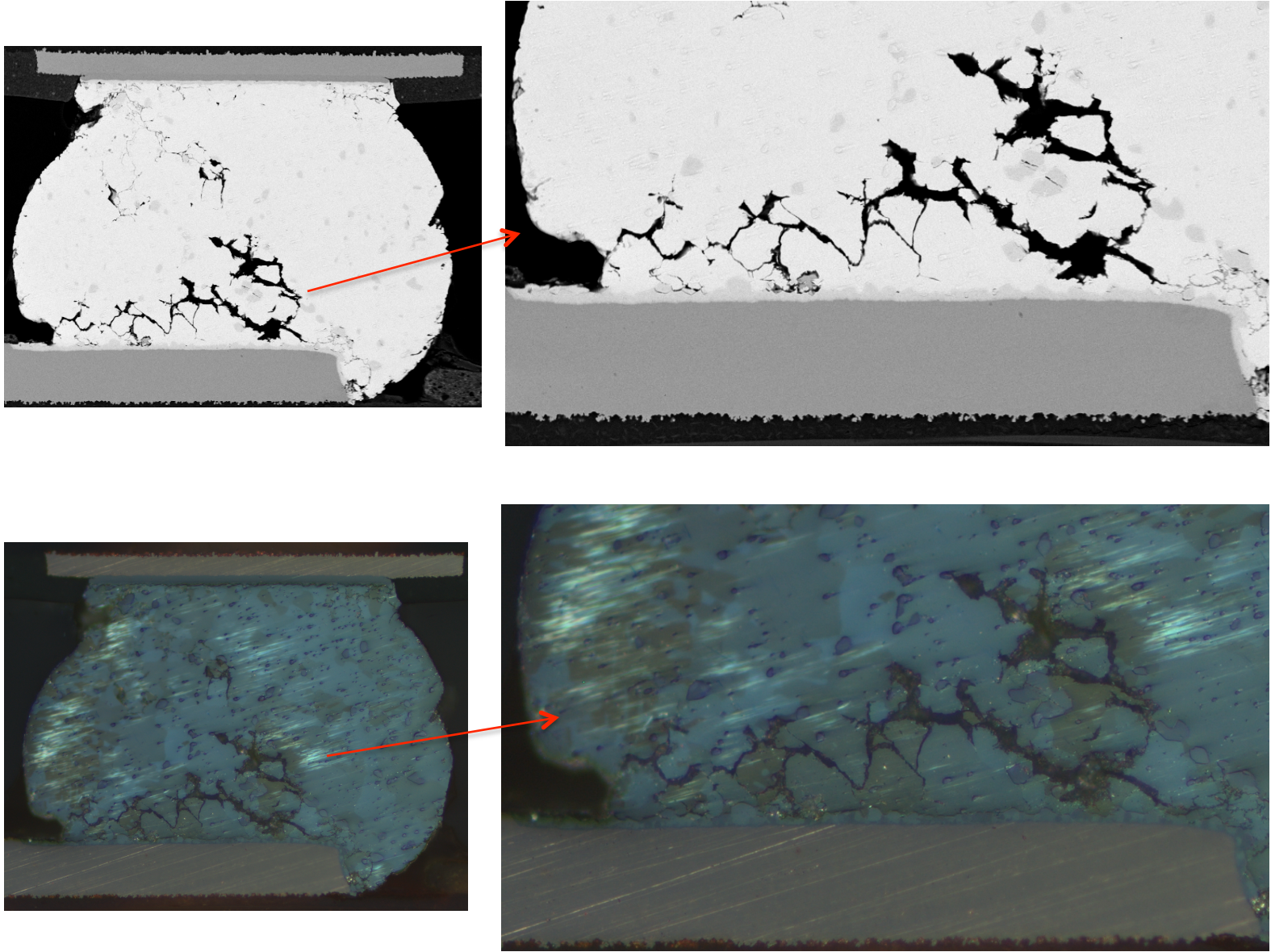


Figure 5.11 Polarized light microscope image with corresponded SEM image for a 15mm BGA solder joint with cracks

Figure 5.11 shows clearly how main the crack and sub-cracks propagate along recrystallized grain boundaries.

Figure 5.12 illustrates a failure mode for 2512 surface mount resistors.

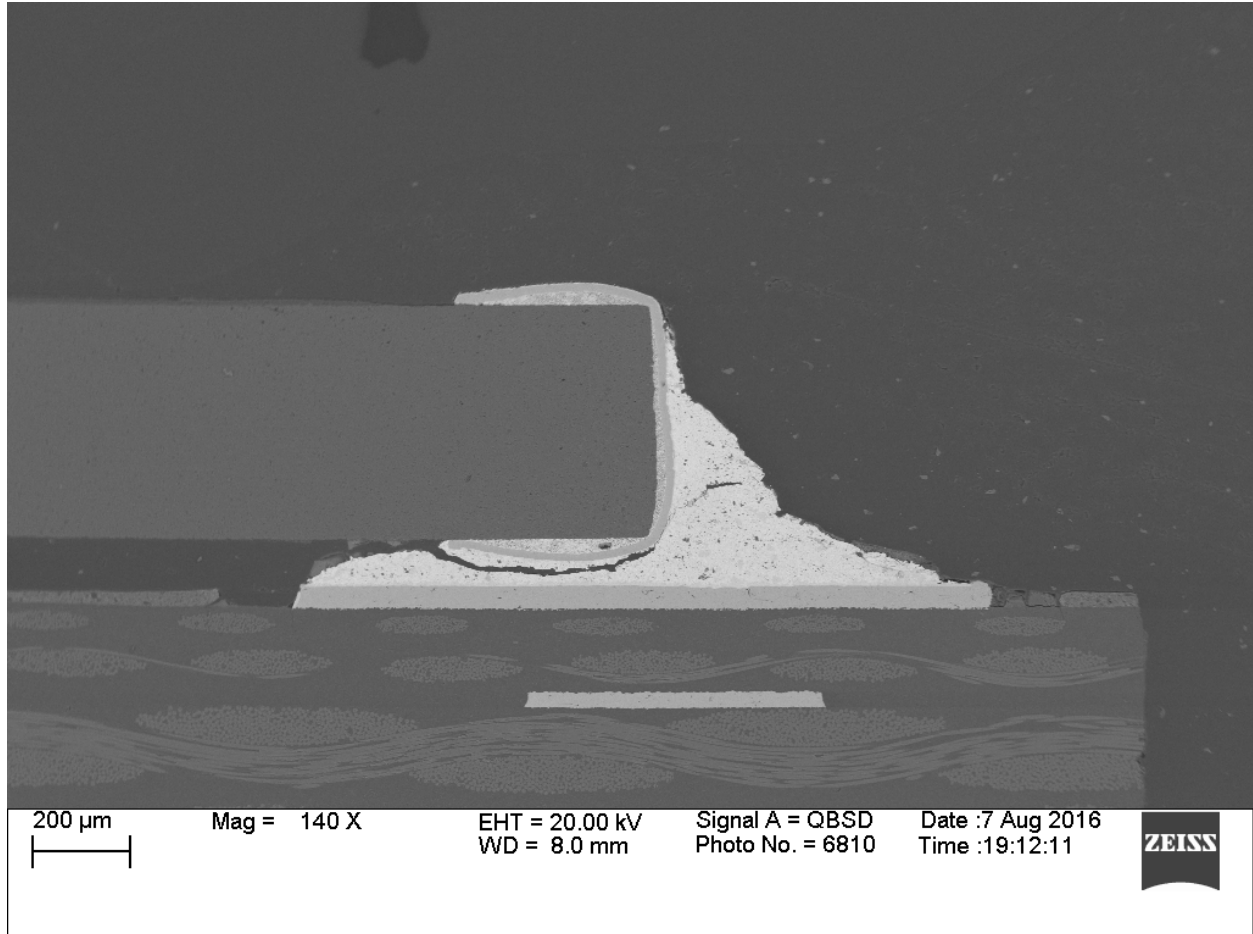


Figure 5.12 Failure mode for 2512 surface mount resistor

From Figure 5.12 we can conclude for 2512 resistor, the crack typically initiates at the inside of the joint and propagates underneath the component termination and then outward through the primary fillet until an open circuit occurs. This is the typical fatigue failure mechanism observed in surface mount resistors. Crack initiation generally occurs in high stress regions, which for surface mount resistors are located beneath the termination.

5.7 IMC Growth and Thickness Analysis

During thermal aging and cycling, the IMC layer in both the component- and board-side interfaces thicken continuously, consuming material from the copper pads and solder joint, and since the IMC layer is brittle, the near-interfacial region is often the principal area in which crack initiation and propagation are observed due to high stress concentration and fatigue. We routinely measure the thickness of the IMC region over time and different pastes because solder joint failure is frequently associated with the extent of IMC formation. Since the thickness is difficult to measure due to the scalloped nature of most IMC films, we average three measurements along the intermetallic layer for three solder balls, located at a left, center, and right corner line under a package.

Table 5.1 shows the total IMC layer thickness growth for a 19mm BGA package with Paste I and OSP finishes with the increasing of thermal cycles. The data in the Table are summarized in Figure 5.13.

Table 5.1 IMC layer thickness growth for a 19mm BGA package with Paste I and OSP finishes

Solder Alloy Thermal Cycles	Paste I SAC305 OSP	Paste I Match OSP	Paste I SAC105 OSP
0	4.9	3.7	4.8
700	7.2	5.5	6.0
1500	7.4	6.8	7.3
2600	7.6	10.1	13.1

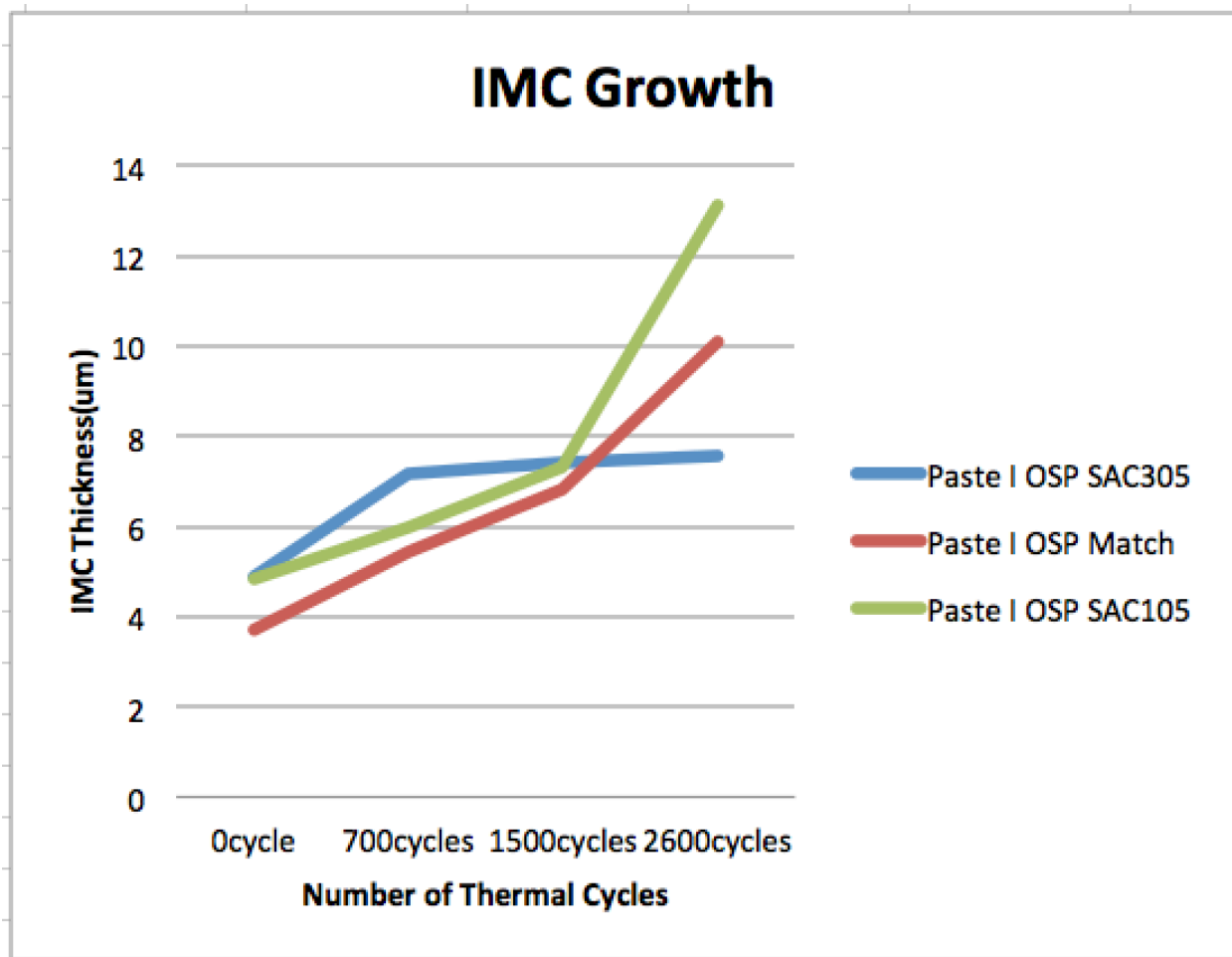
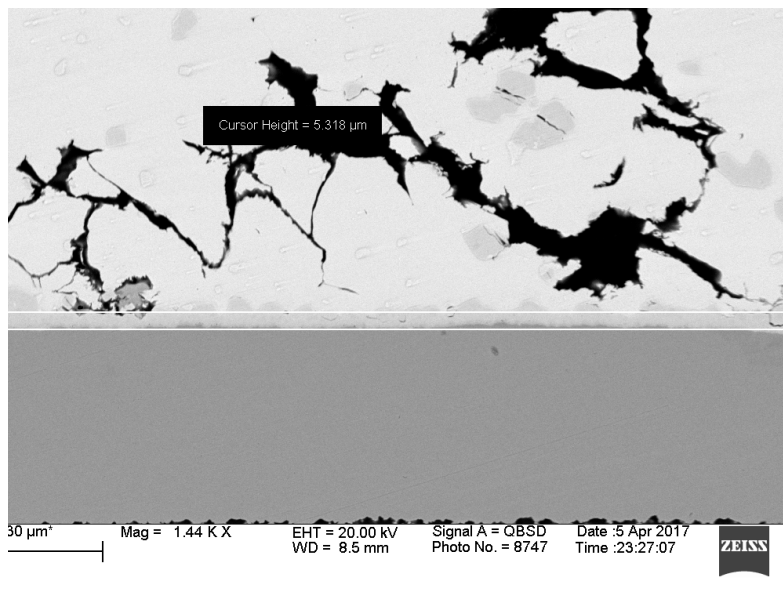


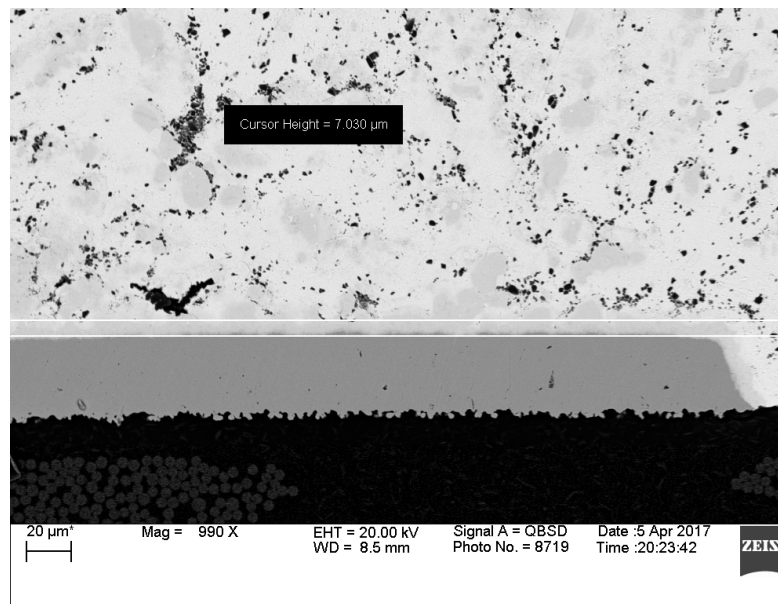
Figure 5.13 IMC layer thickness growth for 19mm BGA package with Paste I and OSP finishes with the increase of thermal cycles

From Figure 5.13 we can conclude that the board side IMC layer thickness for Paste I with OSP finish increases significantly during thermal cycling. At 2600 cycles, for Paste I the BGA packages with SAC105 and matched spheres have a much thicker IMC layer than packages with SAC305 sphere.

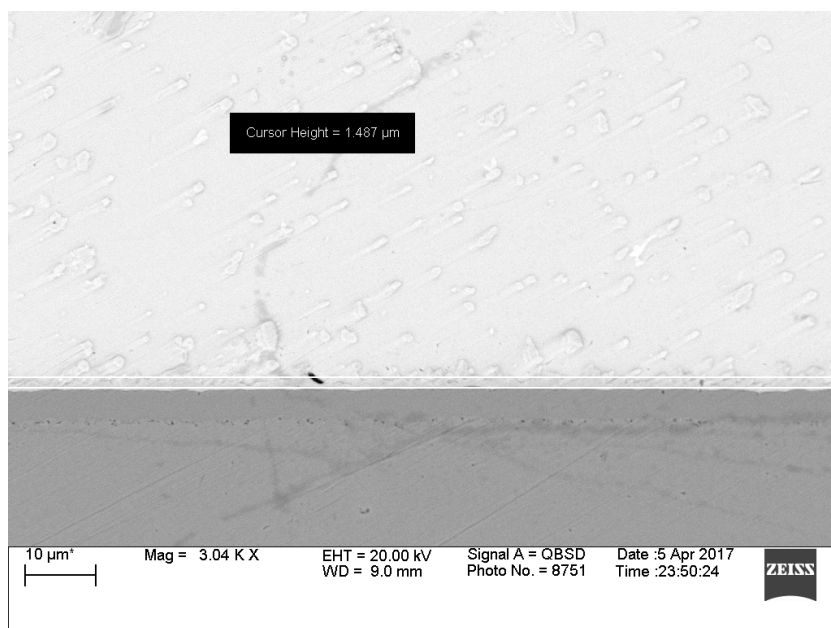
Figure 5.14 shows the comparison of the board side IMC layer thickness at 2600 thermal cycles for Paste A with different surface finishes.



(a)



(b)



(c)

Figure 5.14 Comparison of board side IMC layer thickness at 2600 thermal cycles for Paste A
with: (a) ImAg finish, (b) OSP finish, (c) ENIG finish

From 5.14, we can conclude that the board side IMC layer thickness at 2600 thermal cycles for Paste A with ImAg and OSP finish is 5.31um and 7.03um, respectively. While for Paste A with ENIG finish, the IMC thickness is 1.49um, which is much thinner. This is due to the additional nickel layer between the solder joint and PCB copper pad, which acts as a diffusion barrier preventing copper dissolution into the solder to limit the IMC layer thickness.

The effect of isothermal aging on IMC layer thickness growth is shown in Figure 5.15.

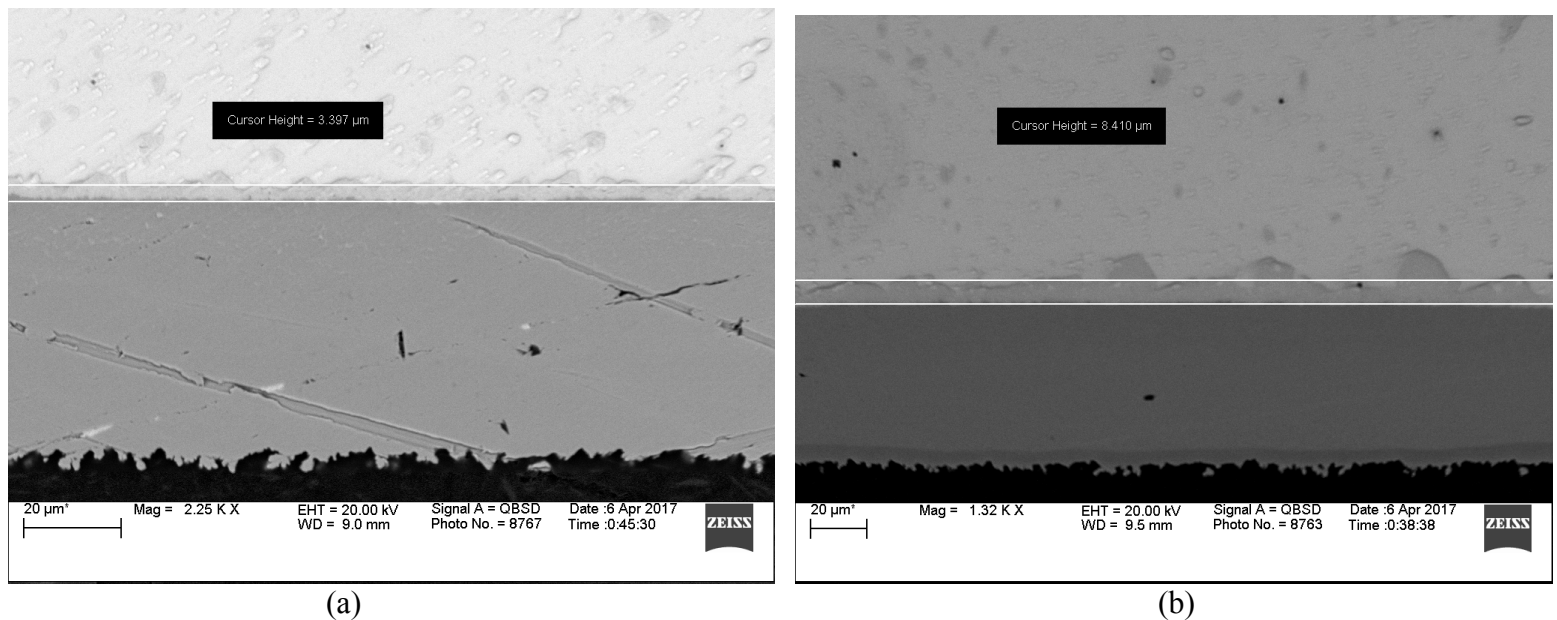
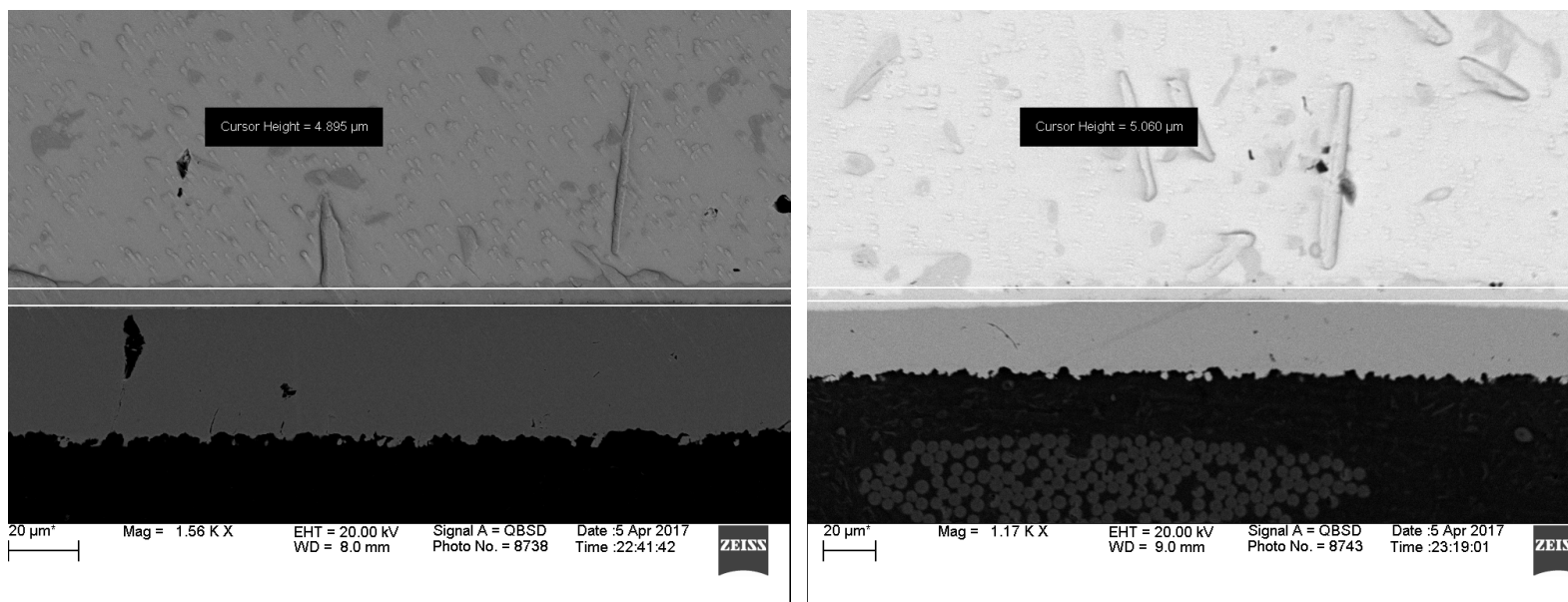


Figure 5.15 Comparison of board side IMC layer thickness for Paste C with: (a) no aging, (b) 12 month aging at 125°C (measured at 2600 Thermal Cycles)

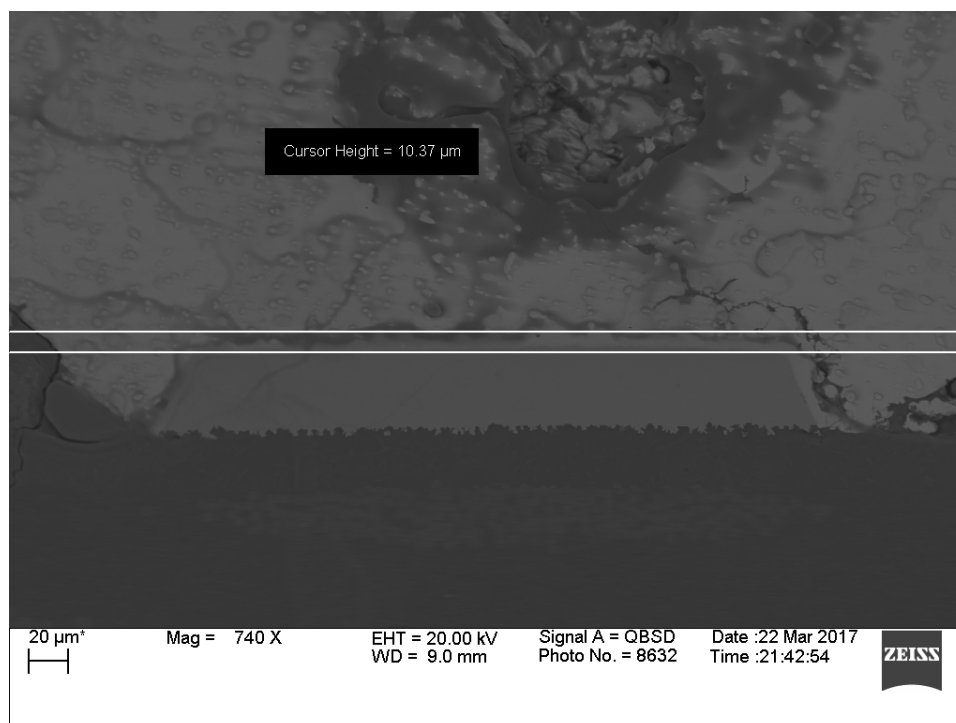
Figure 5.15 shows that the board side IMC layer thickness for Paste A (measured at 2600 Thermal Cycles) increases from 3.397um with no aging to 8.410um with 12 month aging at 125°C, which verifies that thermal aging thickens IMC layer.

Figure 5.16 shows the effect of different dopants on the thickness of IMC layer.



(a)

(b)



(c)

Figure 5.16 Comparison of board side IMC layer thickness for (a) Paste B OSP finish match sphere: (a) Paste F ImAg finish match sphere, (c) Paste I OSP finish match sphere

From Figure 5.16, we can observe that Paste I has a much thicker IMC layer than Paste B and Paste F. Paste I contains no bismuth and less silver than Paste B and Paste F, which contains high bismuth ($>3\%$) and silver ($>3.4\%$). The bismuth and silver content in solder pastes help limit the growth of the IMC layer, as well as prevent copper diffusion from the PCB copper pad into solder joint. The addition of bismuth plus silver helps stabilize the interfacial IMC layer and improves reliability performance.

Chapter 6

Results and Conclusions

6.1 Results and Conclusions

Long-term isothermal aging in elevated temperature has a severe impact on the reliability of SAC solder joints. Two-parameter Weibull plots from previous study shows that the reliability of BGA packages degrades up to 70% after two years of aging at elevated temperature (125°C). With increases in aging time and temperature, the reliability of BGA components degrades more. This dissertation investigates the effect of long-term isothermal aging and thermal cycling on the reliability of lead-free solder mixes with different solder dopants, PCB surface finishes, and isothermal aging conditions. Three surface finishes (OSP, ImAg, and ENIG) were tested in combination with 14 doped solder materials (SAC+ Bi, Sb, Ni, Mn, Nd, and In) and a variety of components. Test vehicles were subjected to isothermal aging (12 months at 125°C) and thermal cycling conditions (-40 to 125°C) in order to evaluate the viability of solder doping for enhancing solder joint reliability. Two-parameter Weibull analysis and failure percentages were generated for data analysis. SEM and polarized light microscope were used for failure analysis, including failure modes, crack propagation, microstructural changes, and IMC layer thickness growth investigation. Data taking as well as sample preparation for this project is ongoing, and until the publication of this dissertation, 2700 thermal cycles have been run. Conclusions at this time are as follows:

(1) Based on the failure percentages at 2700 thermal cycles, 8 doped solder pastes (Paste C, D, K, J, B, E, H, and L) demonstrate superior reliability and are primary candidates for best performance solder paste material, while 4 pastes (Paste A, I, F, and G) have somewhat lower performance. Current failure percentages indicate that, Paste A is the least reliable of all solder

pastes, following paste I, which only performs well with SAC305 solder sphere BGA. Paste F and G also have poor reliability when used with 2515 surface mount resistors and SAC105 solder sphere. Also at 2700 thermal cycles no failures occurred for both 6mm BGA and QFN packages across all test groups, which corresponds to previous research results that a BGA with full array ball arrangement tends to have much higher reliability than a perimeter array. From the composition of all solder pastes we can notice that good performance solder pastes tends to have high Ag content ($>3.0\%$), Bi content ($>3.0\%$), and Sb content ($>1.5\%$). The particle size in solder pastes also influences the reliability of solder joints.

(2) Weibull analysis shows that different solder sphere (SAC105, SAC305, and Matched) and surface finish (OSP, ImAg, ENIG) combinations deliver different solder joint reliabilities.

(3) Weibull analysis also shows that dopants in solder pastes help mitigate the effect of isothermal aging on the reliability of a solder joint. For 15mm BGA package with SAC105 sphere and ImAg surface, applying Paste B can provide an improvement of 68.0% of reliability compared to using SAC305 paste. And for 15mm BGA package with SAC305 sphere and ENIG surface, applying Paste K can have an improvement of 48.5% of reliability compared to using SAC305 paste.

(4) Failure analysis demonstrates that during thermal aging and cycling, the solder joint undergoes deformation due to the CTE mismatch between the solder joint and the PCB and the component, as well as local CTE differences between grains within the solder. Solder microstructural changes include intermetallic compound (IMC) layer growth at PCB/solder joint/package interface or along grain boundaries in the solder bulk and grain coarsening and recrystallization over time and temperature. For solder pastes that contain high silver content, large plate-like Ag_3Sn bulk IMC can usually be noticed, together with particle-like Cu_6Sn_5 bulk

IMC. There are also particle-like Ag_3Sn bulk IMC, with particle size to be much smaller than Cu_6Sn_5 bulk IMC.

(5) Polarized light microscope images show recrystallization phenomenon in the solder bulk, usually with a “beach ball” structure, where different brightness regions in the image indicate different dominant crystal orientations.

(6) Microstructural analysis shows that for the SAC solder system with ImAg or OSP surface finish, the typical interfacial IMC layers are Cu_6Sn_5 and Cu_3Sn at the Sn/Cu interface and Ag_3Sn precipitate in the solder bulk. For SAC solders with ENIG plating, the IMC layer becomes $(\text{Cu}, \text{Ni})_6\text{Sn}_5$ and $(\text{Ni}, \text{Cu})_3\text{Sn}_4$. The presence of the nickel layer in ENIG/ENEPIG acts as a diffusion barrier, which retards Cu dissolution into the solder to insure better reliability.

(7) Crack propagation and failure modes for BGA packages: Cracks in solder joints cause increasing electrical resistance and eventual open circuits in BGA components. Cracks usually initiate from the regions with the largest stresses (corner areas for BGA package), and then propagate following stress distribution. During thermal aging and cycling, the solder joint undergoes deformation due to the CTE mismatch between the solder joint and the PCB and the component, as well as local CTE differences between grains within the solder. The near-interfacial region is often the principal area in which crack initiation and propagation are observed due to high stress concentration and fatigue. Solder recrystallization is also frequently observed in fatigue failures wherein cracks are formed away from the solder interfaces and along the recrystallized grain boundaries within the bulk of the solder at positions where the stress is high. Ag_3Sn bulk IMC can sometimes block the propagation of crack through solder bump, thus pastes with high silver content tends to have higher reliability.

(8) Crack propagation and failure modes for 2512 surface mount resistor package: crack initiates at the inside of the joint and propagates underneath the component termination and then outward through the primary fillet until an open circuit occurred. This is the typical fatigue failure mechanism observed in surface mount resistors. Crack initiation generally occurs in high stress regions, which for surface mount resistors are located beneath the termination.

(9) IMC thickness analysis shows that during thermal aging and cycling, IMC layer in both the component- and board-side interfaces thicken continuously, consuming material from the copper pads and solder joint. Because solder joint failure is frequently associated with the extent of IMC formation, we routinely measure the thickness of the IMC region over time and different pastes. ENIG finish can limit the IMC layer thickness, because it has an additional nickel layer between solder joint and PCB copper pad, which acts as a diffusion barrier preventing copper dissolution into the solder. Solder pastes with high bismuth (>3%) and silver (>3%), can help limit the growth of IMC layer thickness, as well as prevent copper diffusion from PCB copper pad into solder joint, hence help stabilize and strengthen interfacial IMC layer and improve reliability performance.

6.2 Future Work

Since this project is ongoing, more thermal cycles can run continuously until all test vehicles reach complete failure. At that time the best performance manufactureable solder paste with dopants can be finally chosen and verified out of the primary candidates, then the appropriate solder material for solder-sphere replacement can be found for enhancing individual package reliability. Also data and failure analysis can be conducted for 6mm BGA package and QFN package.

In addition to further data and failure analysis, finite element analysis (FEA) model can be developed. FEA models are not necessarily accurate for predicting failure, but they are effective for understanding critical factors of the failure mechanisms. We will collaborate with Dr. Jeff Suhling's research group from the Mechanical Engineering Department of Auburn University for the build of FEA model.

Finally, since this project is designed to investigate the effect of dopants added in traditional SAC solder alloy on the reliability of solder joints under thermal aging and cycling, we are proposing another project to test new solder alloys with dopants that can improve reliability for vibration and drop applications. Our goal is to finally find a “magic paste” that delivers good reliability performance for thermal and drop as well as vibration at the same time, with a reasonable cost.

References

1. Lau, J. H., Wong, C. P., Lee, N. C., and Lee, S. W. R., 2003, Electronics Manufacturing with Lead-Free, Halogen-Free, & Conductive-Adhesive Materials., McGraw-Hill Handbooks.
2. Ray P. Prasad, “Surface Mount Technology Principles and Practice”.
3. Dally, J. W., Lall, P., and Suhling, J. C., 2008, Mechanical Design of Electronic Systems.
4. https://en.wikipedia.org/wiki/Electronic_packaging
5. J. Lau, C. Wong, J. Prince, and W. Nakayama, Electronic Packaging: Design, Materials, Process, and Reliability, McGraw-Hill.
6. R. S. Khandpur, *Printed circuit boards: design, fabrication, assembly and testing*, Tata-McGraw Hill, 2005 ISBN 0-07-058814-7, pages 373–378.
7. Prasad, R., 1997, Surface mount technology: principles and practice., Springer Science & Business Media.
8. Electronic Packaging: Solder Mounting Technologies in K.H. Buschow et al (ed), Encyclopedia of Materials: Science and Technology, Elsevier, 2001 ISBN 0-08-043152-6, pages 2708-2709.
9. Horowitz, Paul; Hill, Winfield (1989). The art of electronics (2nd ed.). Cambridge [u.a.]: Cambridge Univ. Press. ISBN 9780521370950.
10. Williams, Paul, ed. (1999). Status of the Technology Industry Activities and Action Plan.
11. Intel (1996). Packaging. McGraw-hill Inc. ISBN 1-55512-254-X.
12. Montrose, Mark I. (1999). "Components and EMC". EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple. Wiley-Interscience. p. 64. ISBN 978-0780347038
13. IPC, 2007, From Vacuum Tubes to Nanotubes: An Amazing Half Century. The Emergence of Electronic Circuit Technology 1957-2007., IPC - Association Connecting Electronics Industries.
14. M. Arra, D. Xie and D. Shangguan, “Performance of QFP Lead-Free Solder Joints under Dynamic Mechanical Loading”, International Microelectronics And Packaging Society.
15. Bonnie C. Baker, “Smaller Packages = Bigger Thermal Challenges”, Microchip Technology Inc.

16. Ken Gilleo (2003). Area array packaging processes for BGA, Flip Chip, and CSP. McGraw-Hill Professional. p. 251. ISBN 0-07-142829-1.
17. G. Zweig, "BGAs: Inspect the Process not the Product," Circuits Assembly, Feb. 1994.
18. Harper, C. A., 2002, Electronic Assembly Fabrication: Chips, Circuit Boards, Packages, and Components, McGraw-Hill.
19. A. R. Djordjevic, R. M. Biljic, V. D. Likar-Smiljanic and T. K. Sarkar, "Wideband Frequency-Domain Characterization of FR-4 and Time-Domain Causality", IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 43, NO. 4, NOVEMBER 2001.
20. D.A. Benson, R. T. Mitchell, M. R. Tuck, D. R. Adkins, D. Shen, D. W. Palmer, "Micro-Machined Heat Pipes in Silicon MCM Substrates", Microelectronics and Photonics Sandia National Laboratories.
21. Lance Criscuolo, "sing Silicon Contacts to Test and Burn-In FLASH Memory, Microprocessors and FPGA's", Bear Technology.
22. M. Ortolani, M. Leoni, P. Scardi, M. Golshan, "Residual stress profile in ceramic laminates", European Powder Diffraction Conference, EPDIC 10.
23. N. Umbhat, P. M. Raj, S. Bansal, R. Doraiswami, S. Bhattacharya and R. Tummala, "New Package/Board Materials Technology for Next-Generation Convergent Microsystems", Packaging Research Center, Georgia Institute of Technology.
24. C. Coombs, H. Holden, "Printed Circuits Handbook", 2003
25. H. H. Manko, "Solder and Soldering", 2nd Edition, McGraw-Hill, New York, 1979.
26. Harper, C. A., 2002, Electronic Assembly Fabrication: Chips, Circuit Boards, Packages, and Components, McGraw-Hill.
27. Gilleo, B. K., 1994, "The First 7000 Years of Soldering, Part I," (October).
28. Hunt, and LePrevost, "Getting the Lead Out - Soldering with Lead-free Solders.pdf," Proceedings of the RCI 22nd International Convention.
29. Turbini, L. J., Munie, G. C., Bernier, D., Gamalski, J., and Bergman, D. W., 2001, "Examining the environmental impact of lead-free soldering alternatives," IEEE Trans. Electron. Packag. Manuf., **24**(1), pp. 4-9.
30. Davis, J. R., ed., 2001, Alloying: Understanding the Basics, ASM International.

31. S. F. Al-sarawi, D. Abbott, and P. D. Franzon, "A Review of 3-D Packaging Technology", IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY—PART B, VOL. 21, NO. 1, FEBRUARY 1998.
32. J. Bath, "A Manufacturable Lead-Free Surface-Mount Process?", Circuits Assembly JANUARY 2003.
33. NEMI Tin Whisker User Group, —Interim Recommendation on Lead-Free Finishes for Components Used in High-Reliability Products, March 2004.
34. N.C. Lee, "Pb-free Soldering—Where the World is Going," Advancing Microelectronics (Sept./Oct. 1999), p. 29.
35. Cong Zhao, Chaobo Shen, Zhou Hai, Jiawei Zhang, M.J. Bozack, and J. L. Evans, "Long Term Aging Effects on the Reliability of Lead Free Solder Joints In Ball Grid Array Packages With Various Pitch Sizes and Ball Alignments", Proc. of SMTA International 2015, pp 199-206, 2015
36. Zhang, J., 2012, "The Effects of Aging on the Reliability of Lead Free Fine-Pitch Electronics Packaging," Auburn University.
37. N. Socolowski, "Lead free alloys and Limitations for surface mount assembly. Proceedings of Surface Mount International, 1994, pp. 477-480.
38. Handwerker, C., 2002, "Lead-Free Solders : Properties , Processing , Reliability," NIST.
39. Sona, M., and Prabhu, K. N., 2013, "Review on microstructure evolution in Sn-Ag-Cu solders and its effect on mechanical integrity of solder joints," J. Mater. Sci. Mater. Electron., 24(9), pp. 3149–3169.
40. J. DeVore, "Fatigue resistance of solder", NEPCON Proceedings, February 1982, pp. 409-414
41. Cai, Z., Zhang, Y., Suhling, J. C., Lall, P., Johnson, R. W., Bozack, M. J., "Reduction of Lead Free Solder Aging Effects using Doped SAC Alloys," Proceedings of the 60th Electronic Components and Technology Conference, pp. 1493-1511, Las Vegas, NV, June 1-4, 2010.
42. Huang, M. L. and Wang, L., "Effects of Cu, Bi and In on Microstructure and Tensile Properties of SnAg-X (Cu, Bi, In) Solders," Metallurgical and Materials Transactions A Vol. 36(6), pp. 1439-1446, 2005
43. S. F. Al-sarawi, D. Abbott, and P. D. Franzon, "A Review of 3-D Packaging Technology", IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY—PART B, VOL. 21, NO. 1, FEBRUARY 1998.

44. Ford, Michael. "Circuit Assembly Online Magazine - A History of Placement Programming and Optimization". circuitsassembly.com
45. Girouard, Roland. "Mark5 Reflow Oven". Heller Industries Website. Heller Industries Inc.
46. E. Kamen, A. Goldstein, O. Asarangchai, A. Fraser, K. Klatka, J. Belmonte, R. Huber, "Analysis of Factors that Affect Yield in SMT Assembly".
47. T. M. TIRPAK, "Design-to-Manufacturing Information Management for Electronics Assembly", The International Journal of Flexible Manufacturing Systems, 12 (2000), pp. 189–205.
48. Institute of Electrical and Electronics Engineers (1990) IEEE Standard Computer Dictionary: A Compilation of IEEE Standard Computer Glossaries. New York, NY ISBN 1-55937-079-3
49. Bhanu Sood, "Root-Cause Failure Analysis of Electronics", SMTA Philadelphia, March 14, 2013
50. J. Zhang, Z. Hai, S. Thirugnanasambandam, J.L. Evans, M. J. Bozack, "Correlation of Aging Effects on Creep Rate and Reliability in Lead Free Solder Joints", Journal of Surface Mount Technology, (2012), Vol. 25 (3), pp. 19-28 Orlando, FL.
51. Azira N.M.M, N.M Mohd Nan, M.A Idris and M.Z Bukhari, "Board Level Reliability (BLR) - board design, test, and application", ICRAMME 2005, Malaysia
52. M.A. Matin, W.P. Vellinga, M.G.D. Geers. "Thermomechanical fatigue damage evolution in SAC solder joints," Materials Science and Engineering A 445–446 (2007), pp. 73–85.
53. C. Shen, C. Zhao, Z. Hai, J. Zhang, M. J. Bozack, J. C. Suhling, and J.L. Evans, "Sn-Ag-Cu Solder Joints Interconnection Reliability of BGA Package during Thermal Aging and Cycling", Proceedings of the 48th IMAPS, October 2015
54. Zhang, J., Hai, Z., Thirugnanasambandam, S., and Evans, J. L., 2009, "Isothermal Aging Effects on the Dynamic Performance of Lead-Free Solder Joints," pp. 390–397.
55. Zhou Hai, Jiawei Zhang, Chaobo Shen, John. L. Evans and M. J. Bozack, "Long-term Aging Effects on Reliability Performance of Lead-Free Solder Joints", SMTA International 2013, 2013
56. Munshi Basit, Mohammad Motalab, Jeffrey C Suhling, John L Evans, Pradeep Lall, "FEA Based Reliability Predictions for PBGA Packages Subjected to Isothermal Aging Prior to Thermal Cycling", 2015 InterPACK, 2015
57. Aaron Olson, "What are Intermetallics and How Can We Overcome the Failures Associated with Them", STI Electronics

58. Eric Basstow, "Intermetallics In Soldering", Indium Corporation, 11/11/2011
59. Ma H, Suhling JC. A review of mechanical properties of lead-free solders for electronic packaging. *J Mater Sci* 2009;44:1141–58.
60. Jingbo Wan, ongchang, Chen Wei, Zhiming Gao, "Effect of the addition of In on the microstructural formation of Sn–Ag–Zn lead-free solder", *Journal of Alloys and Compounds*, Volume 463, Issues 1–2, 8 September 2008, Pages 230–237.
61. Dhafer Abdulameer Shnawah, Mohd Faizul Mohd Sabri, Irfan Anjum Badruddin. "A review on thermal cycling and drop impact reliability of SAC solder joint in portable electronic products". *Microelectronics Reliability* 52 (2012) 90–99
62. Witoon Kittidacha, Adirom Kanjanavikat, Kamtida Vattananiyom. "Effect of SAC Alloy Composition on Drop and Temp cycle Reliability of BGA with NiAu Pad Finish", 978-1-4244-21 18-3/08 ©2008 IEEE. 2008 10th Electronics Packaging Technology Conference.
63. Richard Coyle, Michael Reid, Claire Ryan, Richard Popowich, Peter Read, Debra Fleming, Maurice Collins, Jeff Punch, Indraneel Chatterji. "The Influence of the Pb-free Solder Alloy Composition and Processing Parameters on Thermal Fatigue Performance of a Ceramic Chip Resistor", 2009 Electronic Components and Technology Conference. 978-1-4244-4476-2/09 ©2009 IEEE
64. T.Y. Lee, W.J. Choi, K.N. Tu, and J.W. Jang: *Mater. Res.* 17, 291 (2002).
65. P. Ratchev, B. Vandevelde, and I.D. Wolf, *IEEE Trans. Dev. Mater. Reliability* 4, 5 (2004).
66. X. DENG, G. PIOTROWSKI, J.J. WILLIAMS, and N. CHAWLA, "Influence of Initial Morphology and Thickness of Cu_6Sn_5 and Cu_3Sn Intermetallics on Growth and Evolution during Thermal Aging of Sn-Ag Solder/Cu Joints", *Journal of Electronic Materials*, Vol. 32, No. 12, 2003.
67. Zhang, L.a, Xue, S.-B.a , Gao, L.-L.a, Zeng, G.a, Sheng, Z.a, Chen, Y.b, Yu, S.-L, "Effects of rare earths on properties and microstructures of lead-free solder alloys", *Journal of Materials Science: Materials in Electronics*, Volume 20, Issue 8, 2009, Pages 685-694
68. Patrick Roubaud, Grace Ng, Greg Henshall, Ronald Bulwith, Robert Herber, Swaminath Prasad, Sundar Kamath "Impact of Intermetallic Growth on the Mechanical Strength of Pb-Free BGA Assemblies", APEX 2001 on January 16-18, 2001 in San Diego, CA
69. Wassink, R. J. Klein, *Soldering in Electronics*, 2nd ed., 1989, Electrochemical Publications Limited, Ayr, Scotland.
70. Che, F. X., and Pang, J. H. L., 2012, "Characterization of IMC layer and its effect on thermomechanical fatigue life of Sn-3.8Ag-0.7Cu solder joints," *J. Alloys Compd.*, 541, pp. 6–13.

71. Luhua Xu and John H.L. Pang. "INTERMETALLIC GROWTH STUDIES ON SAC/ENIG AND SAC/CU-OSP LEAD-FREE SOLDER JOINTS". 0-7803-9524-7/06/©2006 IEEE
72. Microstructure evolution observation for SAC solder joint: Comparison between thermal cycling and thermal storage, M. Berthoua, b, c, , P. Retailleau, H. Frémontb, , , A. Guédon-Graciab, C. Jéphos-Davennel, *Microelectronics Reliability*, Volume 49, Issues 9–11, September–November 2009, Pages 1267–1272
73. O'Conner, P. D. T., and Kleyner, A., 2012, *Practical Reliability Engineering*, Wiley.
74. C. Zhao, C. Shen, Z. Hai, M. Basit, J. Zhang, M. J. Bozack, J.L. Evans, J. C. Suhling, "Long Term Aging Effects on The Reliability of Lead Free Solder Joints in Ball Grid Array Packages With Various Pitch Sizes and Ball Arrangement", *Journal of Surface Mount Technology*, Vol.29 (2), pp. 37-46, 2016
75. Hai, Z., 2014, "Reliability of Lead-Free Electronic Package Interconnections Under Harsh Environmental Conditions," Auburn University.
76. C. Zhao, T. Sanders, C. Shen, Z. Hai, J.L. Evans and M. J. Bozack, "Reliability of Doped Lead-Free Solder Joints Under isothermal Aging And Thermal Cycling", *Proc. Of SMTA International* 2016, pp 599-605, 2016
77. Lau, J. H., 2011, *Reliability of RoHS Compliant 2D and 3D IC Interconnects.*, McGraw-Hill.
78. P. Nemeth, "Accelerated Life Time Test Methods for New Package Technologies", *Electronics Technology: Concurrent Engineering in Electronic Packaging*, 2001, pp. 215-219.
79. Qi, Y., Lam, R., Ghorbani, H. R., Snugovsky, P., and Spelt, J. K., 2006, "Temperature profile effects in accelerated thermal cycling of SnPb and Pb-free solder joints," *Microelectron. Reliab.*, 46(2-4), pp. 574–588.
80. Reza Ghaffarian, "Accelerated Thermal Cycling and Failure Mechanisms For BGA and CSP Assemblies", Jet Propulsion Laboratory, California Institute of Technology, NASA
81. K. C. Norris and A. H. Landzberg, "Reliability of controlled collapse interconnections", *IBM J. Res. Develop.*, May 1969, pp. 266-271
82. V. Vasudevan and X. Fan, *An Acceleration Model for Lead-Free (SAC) Solder Joint Reliability under Thermal Cycling*, 2008 ECTC, May 2008, pp. 139-145.
83. Zhang, J., Hai, Z., Thirugnanasambandam, S., Evans, J. L., Bozack, M. J., Zhang, Y., and Suhling, J. C., 2013, "Thermal aging effects on the thermal cycling reliability of lead-free fine pitch packages," *IEEE Trans. Components, Packag. Manuf. Technol.*, 3(8), pp. 1348–

1357.

84. Zhang, J., Hai, Z., Thirugnanasambandam, S., Evans, J. L., Bozack, M. J., and Sesek, R., 2012, "Isothermal Aging Effects on the Harsh Environment Performance of Lead-Free Solder Joints," SMTA International.
85. Zhang, J., Thirugnanasambandam, S., Evans, J. L., Bozack, M. J., and Sesek, R., 2012, "Impact of Isothermal Aging on the Long-Term Reliability of Fine-Pitch Ball Grid Array Packages With Different Sn-Ag-Cu Solder Joints," IEEE Trans. Components, Packag. Manuf. Technol., 2(8), pp. 1317–1328.
86. Zhang, J., Hai, Z., Evans, J. L., Bozack, M. J., Zhang, Y., and Suhling, J. C., 2012, "Thermal Aging Effects on the Thermal Performance of Lead-Free Fine Pitch Packages," IEEE Trans. Components, Packag. Manuf. Technol.
87. A. Farris, J. Pan, A. Liddicoat, B. J. Toleno, D. Maslyk, D. Shangguan, J. Bath, D. Willie, D. A. Geiger, "Drop Test Reliability of Lead-free Chip Scale Packages", IEEE ECTC, pp. 1173-1180, 2008.
88. J. Lee, T. Hwang, J. Ki, M. Yoo, E. Sohn, and J. Chung, "Study on the Board Level Reliability Test of Package on Package (PoP) with 2nd Level Underfill", IEEE ECTC, 2007
89. Coyle, R. J., Sweatman, K., and Arfaei, B., 2015, "Thermal Fatigue Evaluation of Pb-Free Solder Joints: Results , Lessons Learned , and Future Trends," J. Mater., 67(10), pp. 2394–2415.
90. Zipperian, D., 2011, Metallographic Handbook, Pace Technologies.
91. Buehler, L., 2007, Buehler Sum-Met – The Science Behind Materials Preparation, Buehler.
92. José María Servín Olivares and Cynthia Gómez Aceves. TOF SIMS Analysis for SnxOy Determination on Lead-Free HASL PCBs. SMT Magazine • October 2013 28-44.
93. Z. Hai, "Reliability of Lead-Free Electronic Package Interconnections Under Harsh Environmental Conditions," Dissertation, Auburn University, 2014
94. T.T. MATTILA¹ and J.K. KIVILAHTI. Reliability of Lead-Free Interconnections under Consecutive Thermal and Mechanical Loadings. Journal of ELECTRONIC MATERIALS, Vol. 35, No. 2, 2006
95. Zhang, Yifei, et al, —The Effects of Aging Temperature on SAC Solder Joint Material Behavior and Reliability, Electronic Components and Technology Conference, 2008.
96. Fu, N., Suhling, J. C., Mustafa, M., Lall, P., "Aging induced evolution of the cyclic stress-strain behavior of lead free solders," Proceedings of the ITherm 2016, pp. 737-745, Las Vegas, NV, May 31 - June 3, 2016.

97. Fu, N., Suhling, J. C., Lall, P., "Cyclic stress-strain behavior of SAC305 lead free solder: effects of aging, temperature, strain Rate, and plastic strain range," Proceedings of the 66th IEEE Electronic Components and Technology Conference, pp. 1119-1127, Las Vegas, NV, May 31 - June 3, 2016.
98. W. Liu, Y. Tian, C. Wang, X. Wang, R. Liu, "Morphologies and grain orientations of Cu-Sn intermetallic compounds in Sn3.0Ag0.5Cu/Cu solder joints", Material Letters, 86, pp. 157-160, 2012
99. J. Gong, I.C. Ume, "Nondestructive Evaluation of Poor-Wetted Lead-free Solder Joints in Ball Grid Array Packages using Laser Ultrasound and Interferometric Technique", IEEE Transactions on Components, Packaging and Manufacturing Technology, vol.3, no.8, pp.1301-1309, Aug.2013
100. J. Gong, I.C. Ume, et al. "Non-Destructive Evaluation of Solder Bump Quality Under Mechanical Bending Using Laser Ultrasonic Technique", Journal of Surface Mount Technology, vol. 28, Issue 3, PP15-25, Aug. 2015
101. Lall P, Zhang D, Yadav V, Locker D. "High strain rate constitutive behavior of SAC105 and SAC305 leadfree solder during operation at high temperature". Microelectronics Reliability. 2016 Jul 31;62:4-17
102. Lall P, Zhang D, Yadav V, Suhling J, Locker D. "Effect of Temperature on the High Strain Rate Properties of SAC Leadfree Alloys at Temperatures up to 200° C". Electronic Components and Technology Conference (ECTC), 2016 IEEE 66th 2016 May 31 (pp. 1924-1932). IEEE