3D Simulation of SEU in SiGe HBTS and Radiation Hardening by Design

by

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Abstract

This thesis presents 3-D simulation of Single Event Upset (SEU) in IBM 5HP and 8HP heterojunction bipolar transistors (HBT). SiGe HBT has been attractive for space applications because of its high performance. SiGe HBTs were found robust to displacement damages and total ionizing dose radiation. But recent simulations and microbeam experiments show that SiGe HBTs are prone to single event effects. The simulated data are compared with the charge collection results from the microbeam experiments with adjustment of recombination parameters, fitting to microbeam data was, achieved on some HBTs.In general, charge collection was maximum for a strike at the emitter center and reduced for strikes outside deep trench isolation. The positional dependency of charge collection is studied, particularly regarding the drift and diffusion components. The microbeam strikes are shallow in nature due to overlayer. All charges deposited inside deep trench are collected, making 3-D simulation the only viable way of studying charge collection in SiGe HBTs at present.

The CS junction plays a major role in charge collection. One of the obvious way of radiation hardening is removal of the CS junction. This was done by constructing the SiGe HBT on a buried oxide i.e. the intrinsic part of the device is identical to the bulk HBT and CS junction is replaced by the buried oxide. Various simulations were performed for different Si thickness above the buried oxide. It was found that the thickness variation did not have any impact on the charge collection. It was found that the charge collection is much reduced in the SOI HBT. The charge collection in SOI HBT is compared with the bulk HBT. The comparison shows that the charge collected by the collector and substrate are much smaller in SOI than bulk HBTs. But the charge collected by the emitter and base are identical in SOI and bulk HBT. This type of radiation hardening is called as Radiation Hardening By Process (RHBP), as changes in fabrication process, are made.

Another type of radiation hardening is Radiation Hardening By Design (RHBD), where the changes are made in the layout only. In this work we introduce an extra shared dummy CS junction outside the deep trench. This dummy CS junction reduces the diffusive charge collected by the HBT. Design rules require a minimum distance between deep trenches of adjacent devices. The dummy collector can be filled in these space between devices. The charge collection between the bulk and dummy collector device are studied. Also the charge collection characteristic when the devices are introduced into a HBT array is studied. Charge collection in a regular 2×2 and 3×3 HBT arrays are studied. The charge collection is compared between the regular and hardened HBT arrays. It has been found that the dummy CS junction reduces the diffusive charge collection by a considerable amount thereby preventing simultaneous charge collection in multiple devices in a HBT array. The amount of charge collected by the struck device in a HBT array decreases with increasing number of adjacent devices due to the sharing of charge collection. This decrease in charge collection by the struck device becomes very gradual eventually.

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Chapter 1

Introduction

1.1 Motivation

The earth's atmosphere houses a family of communication satellites, which relay signals from one part of the globe to another. Each satellite hosts an enormous amount of electronic circuits. The operation of the electronic circuits in space presents a host of challenges for device, circuit and system designers. The circuits are subjected to harmful radiations which may disrupt the performance of the circuit temporarily or may even destroy the circuit permanently. Advances in fabrication technology have led to the miniaturization of device sizes. As the device size decreases, there is a high probability of malfunction of the device in space. So it is necessary to study the degrading effects of radiation on electronic circuits.

Silicon Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) technology has become an important semiconductor technology for both wired and wireless application because of its superior analog and RF performance, together with its CMOS integration capability [1]. The radiation effect of SiGe HBT technology is of interest to spacecraft designers to insert the latest technology into the system. Clearly, a space qualified IC technology must demonstrate sufficient radiation immunity to support high-speed circuit applications as well possess total dose tolerance. SiGe HBT technology has generated considerable interest in the space community due to its robustness to total ionizing dose radiation (TID) without any additional hardening. But, recently, high speed SiGe HBT digital logic circuits were found to be vulnerable to SEU [2] [3]. Hence it is important to study the Single Event Effects (SEE) on SiGe HBTs. To understand SEE in SiGe HBTs, one must use calibrated three dimensional (3-D) device simulation to assess the charge collection characteristics of SiGe HBTs. It is not only important to study the charge collection characteristics but also propose layouts to radiation harden the devices and circuits.

Radiation Hardening By Design (RHBD) employs layout and circuit architecture changes for the radiation hardening of space electronics systems using commercial foundry processes, with no modifications to the existing process or violation of design rules [4] [5] [6]. Lots of design approaches are proposed for radiation hardening of the devices and circuits. The conventional design procedures are changed in the process or layout to have a radiation hardened end product. As SiGe HBT logic circuits are vulnerable to SEE, it is necessary to change the fabrication process or change the layout to harden the SiGe HBT against SEE.

1.2 Silicon Germanium HBT - What Makes it Special

The SiGe HBT has a different device physics from the Si BJT due to the presence of Si-SiGe heterojunction in the emitter-base and collector-base junction. Introducing Ge into Si effectively decreases the bandgap.

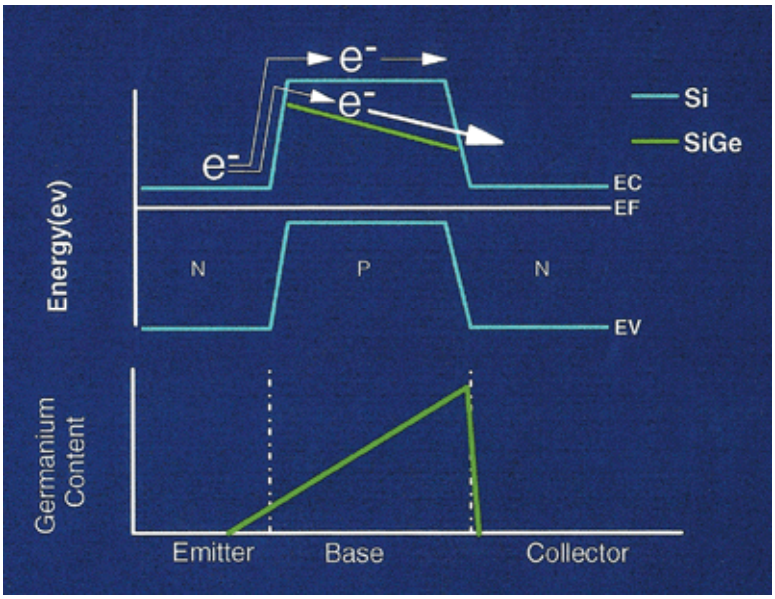


Figure 1.1: Energy band diagram of a graded-base SiGe HBT as compared to an identically constructed Si BJT [8].

The overlaid band diagram for both SiGe HBT and Si BJT are shown in Fig. 1.1. The grading of Ge in the neutral base gives rise to a drift field in the neutral base that will have an impact on

the minority carrier transport in the base. Introduction of Ge into the base increases the collector current density (J_C) due to the increased electron injection in the EB junction. This increased electron injection yields more emitter to collector charge transport for a given EB bias. An increased collector current density yields higher current gain β. The SiGe HBT has a planar self-aligned structure. The SiGe HBT has a poly emitter contact, silicided extrinsic base and deep and shallow trench isolations. The SiGe base is grown using ultra-high vaccum/chemical vapor deposition (UHV/CVD). The n-p-n layers of the intrinsic transistor and the p-type substrate form an n-p-n-p multilayer structure, making the charge collection more complicated. Fig. 1.2 shows a schematic device cross section of a first-generation (50 GHz) SiGe HBT [7].

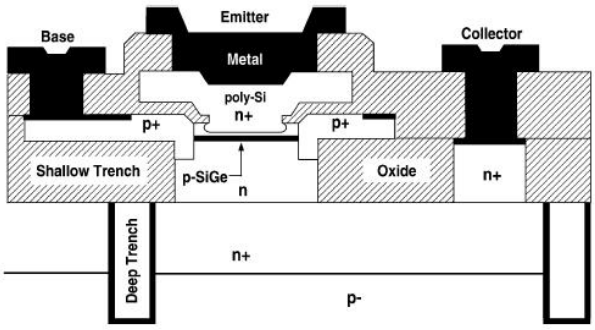


Figure 1.2: Schematic device cross section of a first-generation SiGe HBT [7].

1.3 Single Event Upset

Space is comprised of highly energetic particles. When these energetic particles hit the sensitive nodes of the electronic circuit, it leaves a trail of electron/hole pairs. These charges are collected by the sensitive node of the circuit, which gives rise to Single Event Effect (SEE). This strike may cause a temporary disturbance in the circuit operation or may even cause a permanent damage in the circuit. The single event effects can be classified into two categories. They may be either destructive SEE or non-destructive SEE. Single event current transients (SET) and

single-event upset (SEU) in logic or memory circuits are examples of non-destructive SEE and single-event latchup (SEL) is an example for destructive SEE.

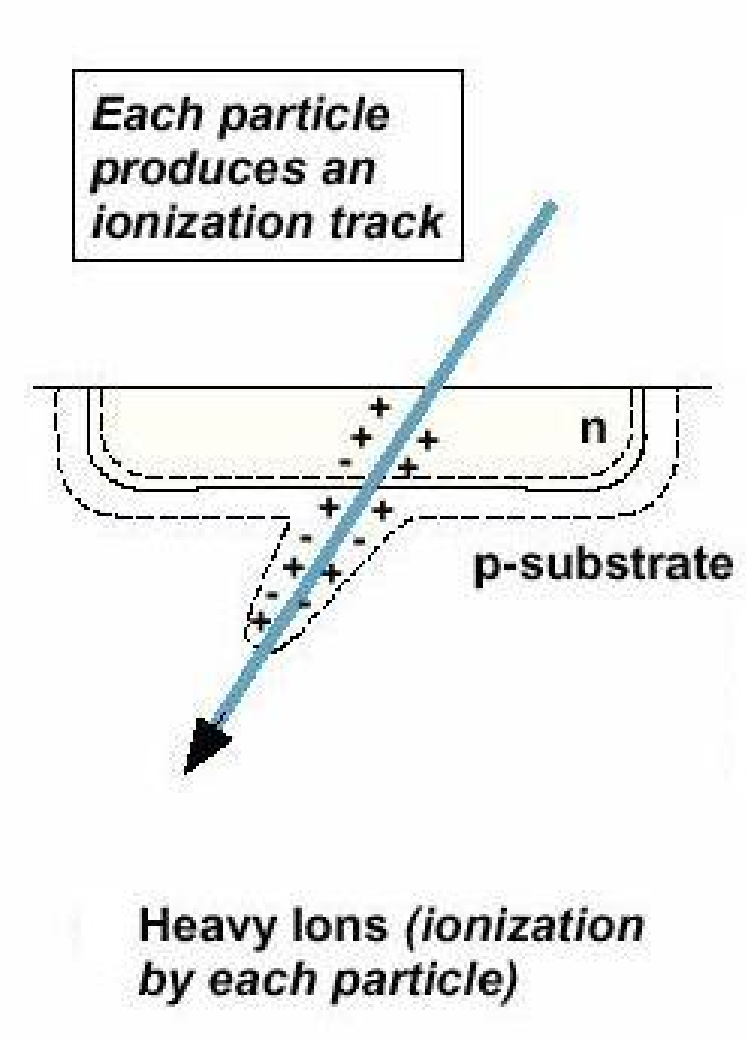


Figure 1.3: Illustration of SEU in a pn junction [10].

When an energetic particle passes in a microelectronic device, there is collection of charge in the sensitive region of the circuit. This mechanism is responsible for all the non-destructive SEE. When an ionizing particle passes through the target material, electrons and holes are released along the path of the ionizing particle. The width of this track depends on the energy of the carriers,

which depends on the energy of the incident particle. Fig. 1.3 illustrates the single event upset in a pn junction. There are two mechanisms of charge generation. In the first type the primary ion generates enough electron/hole pairs to cause an upset which is shown in the figure. In the second type the primary ion has no enough energy to generate the required amount of charge to cause an upset. But the primary ion reacts with the target material to produce secondary ions which can generate enough charge to cause an upset. This thesis addresses only the case where only primary ion generates the charge. Fig. 1.3 shows the formation of carriers along the ion path. The electrostatic potential is disturbed in the junction and this disturbed field extends deep in the substrate. The disturbed field collects charge deposited deep in the substrate [9].

1.4 Radiation Performance of SiGe HBTs

The response of SiGe HBTs to a variety of radiation types has been reported. Device and circuit simulations are required to aid in the search of effective SEU mitigation approaches. Transistor charge collection characteristics are studied as a function of terminal bias, load condition, substrate doping and ion strike depth. The collector-substrate (CS) junction plays a major role in charge collecion in SEU. As explained in the previous section, the CS junction is responsible for the instantaneous charge collection through drift mechanism. Charges generated beyond the CS junction diffuse towards the CS junction and eventually gets collected by the CS junction. The diffusion of the carriers towards the CS junction depends on the substrate doping and the geometry of the device. The deep trench isolation (DTI) mitigates the diffusion of charges, which are generated beyond the silicon island surrounded by the deep trench. Charges can be generated beyond the DTI in two instances: Either the heavy ion strike might occur outside the DT or the strike can be an angled strike where the track can pass both through the silicon island inside and outside DT.

Substrate doping plays an important role in charge collection. Lots of literature work has been done to study the dependence of charge collection characteristic on the substrate doping. The charge collected by the collector terminal of the transistor reduces as the substrate doping increases, which is due to the decreased lifetime of the carriers. Substrate engineering is a major

research topic in space oriented applications. A back junction was introduced in the substrate by introducing a n^+ layer below the p-type substrate. This back junction reduces charge collection by limiting the potential funneling to within the p-layer, thus reducing the drift charge collection. The path of diffusion charge collection is also cut-off by the back junction. A charge blocking buried layer of heavily doped p-type silicon is introduced at the bottom of the DTI. This p^+ layer mitigates the charge collection from events occuring outside the DTI. The above techniques require process changes, which are termed as *Radiation Hardening By Process (RHBP)*.

There is another type of radiation hardening termed as *Radiation Hardening By Design (RHBD)*, where the changes are made in the layout without any changes in the process. The RHBD can be done in the circuit level and device level. At the device level, RHBD C-B-E SiGe HBTs with single collector and base contacts and significantly smaller deep trench-enclosed area than standard dual collector and base contacts to reduce the upset sensitive area. Circuit-level RHBD techniques include dual-interleaving and gated feedback that achieve SEU mitigation through local latch level redundancy and correction. Register level RHBD based on triple-module redundancy (TMR) versions of dual-interleaved and gated-feedback cell shift registers is realized to gauge the performance improvement offered by TMR [12].

1.5 Thesis Contributions

The major SEU inducing particles in microcircuit devices are the cosmic rays. The cosmic ray ions are typically the most energetic species in the nuclear particle physics. The incident cosmic ray ions usually cause soft errors which merely upsets the informational charge state of the sensitive node of a memory cell. The major source that simulate cosmic ray ions that produce SEU are high-energy accelerators. These high energy accelerators are used to get experimental data. The simulated data's validity can be checked through comparison with the experimental data. Chapter 2 gives a detailed discussion of the simulation approach followed in this thesis. IBM SiGe HBT technologies are discussed. Some important SEU jargons are explained in this

chapter. The simulated data is compared with the experimental data obtained from Sandia National Laboratories. A brief detail of the accelerator experiments is given.

When a heavy-ion strikes a device, the CS junction plays a major role in charge collection. If the ion strike path disturbs the CS junction the disturbed potential in the junction collects the charge through drift process. For a strike that does not disturb the CS junction, the charges diffuse towards the CS junction and then get collected by drift mechanism. Chapter 3 gives a detailed explanation of the charge collection processes in SiGe HBTs. A natural way of radiation hardening is to remove the CS junction. This can be done by introducing a buried oxide in the place of the CS junction. This is an example for Radiation Hardening By Process (RHBP), where the process is changed. The charge collection is studied for various thickness of the Si film above the buried oxide. The charge collection is studied for varying loads in the collector terminal. Finally the charge collection of the SOI is compared with the bulk structure. The SOI structure reduces the charge collection through drift and diffusion.

Ion strike occurs in all possible angles in space. Chapter 3 deals with ion strikes occuring at normal incidence to the device surface. The normal strike charge collection characteristics is different from the angled strike charge collection. The positional dependence of charge collection is studied by varying the position of ion strike. The charge collection characteristics at each point is studied for four different angles: normal strike, 30°, 45° and 60° strike. It was found that the worst case charge collection occurs for normal strike. The area of maximum charge collection reduces and the area of minimum charge collection increases as the angle of strike increases. The substrate doping effect on charge collection is studied. Circuits contain multiple devices located adjacent to each other. The charge collection is shared among multiple devices in circuits, which can give rise to multiple bit upsets. Simultaneous charge collection is studied by simulating normal and angled ion strikes in 2x2 and 3x3 array of SiGe HBTs. The amount of charge collected by the struck device decreases with the increasing number of adjacent devices due to charge collection sharing. The decrease in charge collection by the struck device becomes very gradual eventually.

In chapter 3 radiation hardening was acheived through process modifications. The RHBP process is susceptible to low volume concerns such as yield, process instability and high manufacturing costs. In Radiation Hardening By Design (RHBD) changes are implemented either in the layout or in the application architecture and not in the fabrication process. Why RHBD when there is RHBP? The RHBD approach gives a low cost solution, which is a main concern in industries. A new RHBD technique is studied in chapter 4. In this RHBD technique a dummy CS junction is introduced outside the deep trench isolation (DTI). This dummy CS junction surrounds the DTI. This dummy junction is obtained by pulling out the NS layer in the regular HBT. The dummy junction is seen to play a major role in reducing the diffusive charge collected by the CS junction in the regular HBT. The next question to be answered is whether there is any area penalty? In circuits, devices are separated from each other by a certain distance, as laid out by design rules and specifications. These spaces between devices can be filled with the dummy collector. In this chapter multiple devices layout with the dummy CS junction has been simulated for a 2x2 and 3x3 HBT array and is compared with the regular HBT arrays. It is seen that the dummy CS junction prevents charge collection in multiple devices.

Chapter 6 deals with the upset phenomenon in circuits using SiGe HBT. Quasi mixed mode simulations are done to study the upset phenomenon in circuits, where the device level simulation results are coupled to circuit-level modeling to understand the circuit-level SEU. In this chapter true mixed mode simulations are done where the struck device is modeled in device level and all other devices use the gummel-poon model. Quasi mixed mode simulations are compared with true mixed mode simulations for a master-slave d-flipflop. Mixed mode simulations are done on analog emitter follower. In this circuit the collector is at the supply voltage and the emitter is at a lower potential. There is a shunt of the collector and emitter terminal and the shunt current flows from high potential to low potential. The collector to emitter shunt current during SEU is more complex than the collector current itself. Due to the complex nature of this circuit, true mixed mode simulations are required. True mixed mode simulations capture better the device/circuit interactions.

Chapter 2

Simulation Approach

This chapter gives a detailed discussion on the simulation approach followed in this research. The mechanisms of charge collection after a heavy-ion strike is discussed in detail. The world of SEU has lots of jargons involved, which are explained in this chapter. Any device simulation starts with the construction of the device. Device construction in 2-D is not very difficult but it is very involved in 3-D. Hence the device construction technique is explained in detail. The physical models used in the simulation are explained. A detailed discussion on the microbeam experiments are presented and a comparison between the experimental and simulated data is given.

2.1 Construction of the Device

The first step in device simulation is the construction of the device. The devices built in simulation are approximations of the devices used in circuits. The first step in device simulation is the specification of the material boundary of the device. The specification of material boundaries in a 3-D device is more involved than the 2-D construction of the device. In the 3-D construction extra care should be taken to avoid the encroachment of one material into another or to avoid void spaces in the device.

Now the boundary of the device completed, the second step in device construction is the specification of the doping profile and Germanium mole fraction in the base. The vertical cross section of the device consists of an n^+ polysilicon emitter(E), a p-type epitaxial base(B), an n-type collector(C), an n^+ buried layer and a lightly doped p-type substrate. They are obtained from Secondary Ion Mass Spectrometry (SIMS) data. The SIMS data is the doping profile along the center of the device(center of emitter). No SIMS data is available for other points. This data file contains data in xy format with x representing the depth from the surface of the device and

y representing the corresponding doping profile. When specifying the doping profile for the 3-D structure a reference surface is given, which is the surface of the device in our case. The first data in the SIMS file corresponds to the doping at the surface of the device (Reference Surface). The second data corresponds to the depth from the surface of the device with the corresponding doping data at that depth and it goes on. The SIMS has no information on the n^- collector doping and p^+ extrinsic base doping. They are estimated from the fabrication process information.

Simulations are performed on the IBM 5HP and 8HP SiGe HBT which are constructed using the synopsys TCAD tool MESH [13]. The step by step construction of the 8HP HBT is shown below. The technique used in the construction of the 5HP SiGe HBT is similar to that of the 8HP SiGe HBT.

The device construction contains two steps

- Boundary construction
- Doping Specification

The device is divided into layers and each layer is divided into vertical divisions showing the materials in each layer. The horizontal view of the materials in a layer can be seen with a layout of the device. The 3D device is constructed based on the layout and the vertical divisions of the device.

2.1.1 Boundary Construction

Fig. 2.1 gives the schematic cross section and the layout of the regular 8HP device. The regular device is constructed as in the IBM HBT structure without any changes in the layout (RHBD) or process (RHBP). The figures are not drawn to scale. The NS layer defines the N^+ subcollector of the device. The silicon area inside DT determines the collector-substrate (CS) junction area. The device structure can be divided into five layers as seen in the figure. The bottom layer consists of silicon substrate only. The fourth layer consists of the deep trench oxide and silicon and it can be called as the deep trench (DT) layer. The middle layer consists of the shallow trench and

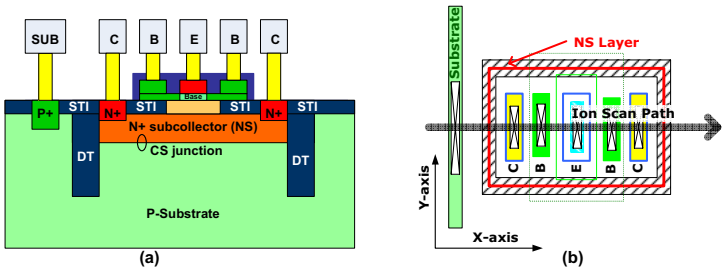


Figure 2.1: (a) Schematic cross-section and (b) schematic of the layout of a SiGe HBT (not to scale).

silicon and is called as the shallow trench (ST) layer. The SiGe layer is on the top of the ST layer. Above the SiGe layer lies the polysilicon emitter. The thickness of each region is determined from the cross section obtained from the Transmission Electron Microscopy (TEM). The boundaries of different regions in 2D can be specified as polygons or multiple rectangles. In 3D, the devices can be constructed with polyhedrons or cuboids. The disadvantages with polyhedron boundaries are

- There is a high probability that we might not get accurate material boundaries in polyhedron specification.
- Polyhedrons are complex to visualize.
- Specifying a polyhedron is a laborious job.
- In polyhedrons we first specify surfaces in a single plane and then we join the surfaces. There is a high probability of specifying points on different planes for a single surface. This might give void regions in the device.

The device is constructed using layers of cuboidal blocks. The first layer is a block of silicon. So we use one cuboidal block to construct the first layer. The cuboidal block is constructed by specifying the opposite ends of the body diagonal of the cuboid. The second layer is the DT layer. The limitations in specifying cuboidal blocks are

- The structure has to be planar.

- It has to be regular layer by layer.
- No corners in real devices can be accounted for in this type of device boundary construction.
- For charge collection the primary concern is the collector-substrate junction, where the simplified regular cuboidal block building approach does not cause significant error.

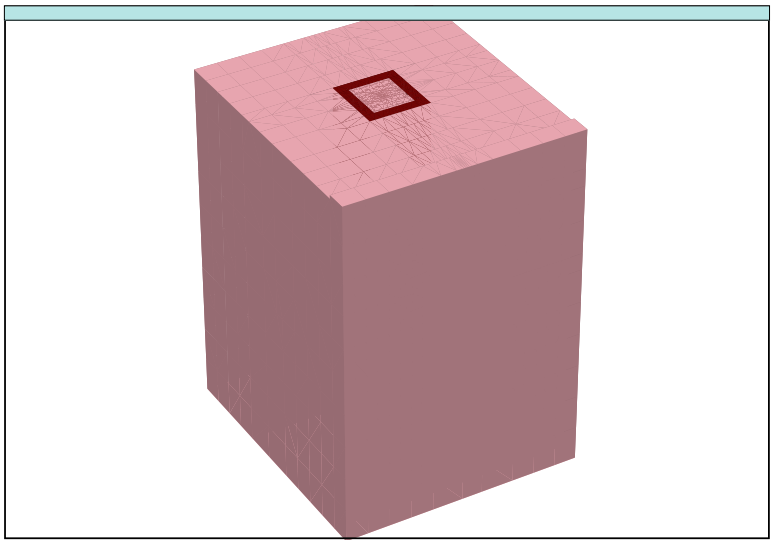


Figure 2.2: The second layer (DT layer) in the device.

Fig. 2.2 gives the DT layer of the device. The brown color is the oxide and the pink color is silicon. The DT layer contains several cuboids containing oxide and silicon. The layout of the DT layer contains multiple rectangles. Each block of the rectangle comprises of a particular material like silicon, oxide etc. Each cuboidal block is specified by two points of the body [X_{min}, Y_{min}, Z_{min}] and [X_{max}, Y_{max}, Z_{max}]. The code can be seen in the appendix. The DT oxide is constructed with four cuboidal blocks. Fig. 2.3 shows the third layer in the device, which is the ST layer. The ST layer is constructed using the same strategy as the DT layer.

The SiGe layer is on top of the ST layer as shown in Fig. 2.4. The extrinsic base is raised in the 8HP HBTs. On top of the SiGe layer is the polysilicon emitter. The extrinsic base is separated from the polysilicon emitter by oxides called as spacers. The spacers surround the emitter. The

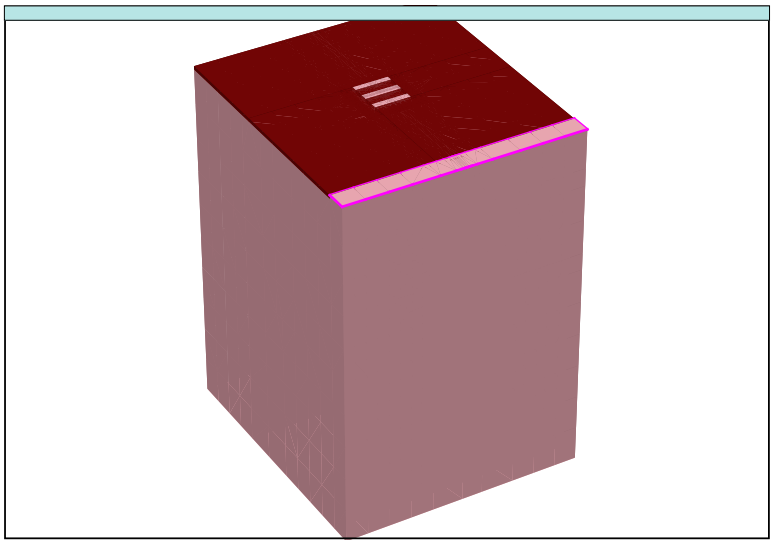


Figure 2.3: The third layer (ST layer) in the device.

emitter has dimensions of 0.12×3.00 μm^2. Fig. 2.5 shows the 3D view of the materials in the device. In the figure we can clearly see the emitter, base, collector and substrate contacts.

2.1.2 Doping Specification

The doping profile is got from the SIMS data. Fig. 3.1 gives the 3-D view of the regular 8HP HBT device. The color indicates the doping profile. The dark red indicates the heavy n-type doping and the dark blue indicates the heavy p-type doping. The center contact is the emitter contact and the two contacts on either side of the emitter are base contacts. The dual collector contacts are on either side of the base contacts. The device is a dual base, dual collector contact device.

A 2-D cut is made along the center of the emitter to get the detailed view of the intrinsic portion of the device. Fig. 2.7 shows the resulting 2D cross section. The device has a p-type substrate. There is the N^+ buried layer, which is the N^+ subcollector (NS) of the regular HBT. This layer is heavily doped to reduce the collector resistance. The collector of the HBT is the selectively implanted collector (SIC). In this type of collector, the portion of the collector under the emitter has the required doping. The region of collector surrounding the emitter has a lower doping. The higher doping under the emitter is to reduce the base-widening effect. The low

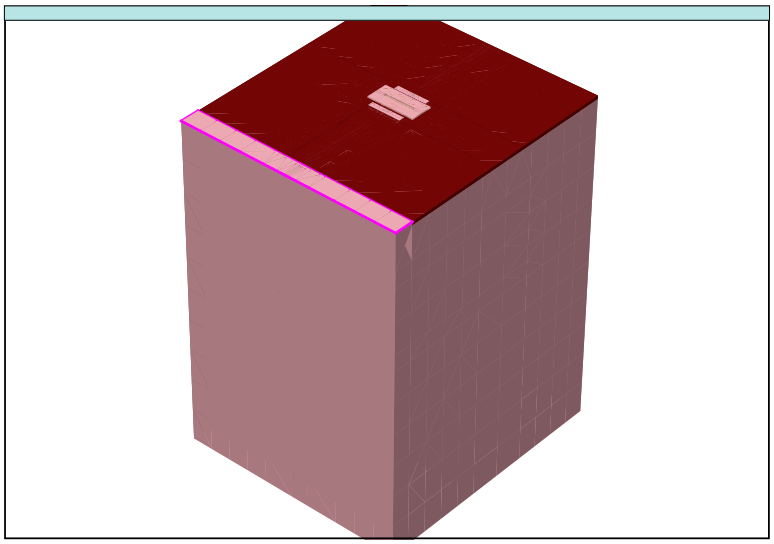


Figure 2.4: The SiGe base layer in the device.

parasitic-collector doping is to reduce the base-collector junction capacitance. SIC is obtained by selective ion implantation. The base contact is made at the raised extrinsic base which is a heavily doped p-type. The heavy doping of the extrinsic base is required to reduce the base resistance. The encroachment of the extrinsic base doping into the intrinsic base should be avoided. If the extrinsic base encroaches into the intrinsic base, then the encroached intrinsic base would appear wider and more heavily doped than the intrinsic base. Deep trench isolation is used to isolate the HBT from nearby devices. Hence the deep trench should be deep enough to isolate the sub-collectors of adjacent transistors. The depth of the deep trench is 8 μm, which is got from the cross section of the device. The collector-substrate junction area is defined by the spacing between the inner deep trench edges.

The 5HP HBT with emitter dimension 0.5 × 10 μm^2 is constructed similarly. Fig. 2.8 shows the 3D view of the 5HP HBT. A cross section at the center of the emitter gives Fig. 2.9. The green color on the two sides of the sub-collector are the deep trench oxide. The difference between the 8HP and 5HP are

- 8HP has a raised extrinsic base while 5HP does not.

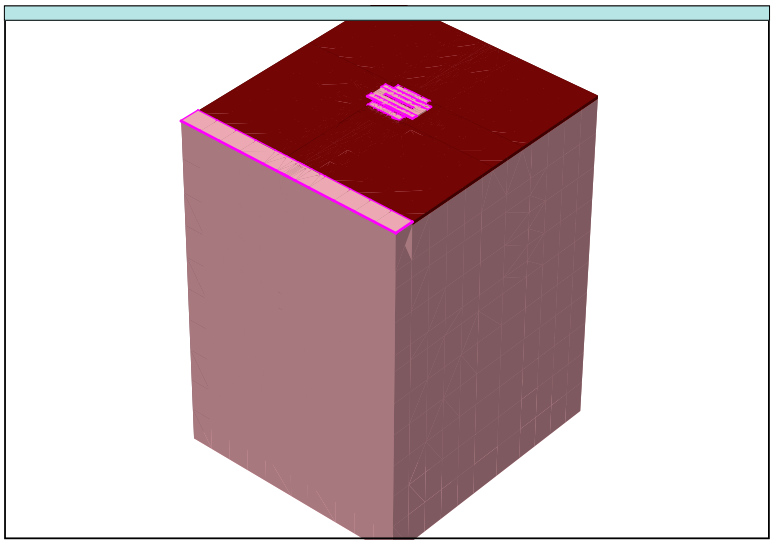


Figure 2.5: The boundary of the device with different materials.

The doping for the intrinsic device is given by the SIMS file. The SIMS file is in xy format, where x is the depth from the device surface and y is the corresponding doping. The lateral doping profile and the doping transition from the intrinsic to extrinsic device is obtained from the device layout and fabrication details. The emitter, base, collector and sub-collector doping profiles are got from the SIMS data. The first data in the SIMS file corresponds to the doping at the surface of the device. A reference plane (Rectangle) is specified, which corresponds to the first data in the SIMS file i.e.the first y-data corresponds to the doping in the reference plane. Each x-data from the second row corresponds to the depth from the reference plan and the y-data corresponds to the doping profile in the corresponding depth. The SIMS data for the substrate contact doping was not available. Hence the substrate contact doping was obtained from the fabrication details. The location of the substrate contact in the device is got from the layout details. The p-well outside the deep trench is defined by a different mask, else we will have a floating $N^{+}P$ junction. Any floating junction in device design is bad for the performance of the device.

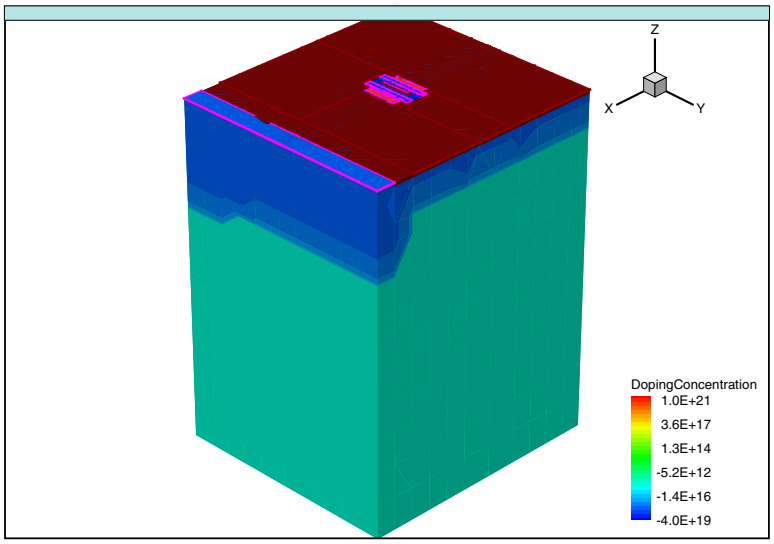


Figure 2.6: 3-D View of the 8HP regular HBT. Color indicates doping profile.

2.2 Device Simulation Parameters

In a device simulation three basic variable, the potential Φ, the electron concentration n and the hole concentration p are solved. The variation of these variables is extensive in p/n junctions of the device. DESSIS uses default parameter values in the parameter files unless specified.

2.2.1 Linear Energy Transfer

When a heavy ion passes through a semiconductor material, it keeps losing energy along its path. Depending on the energy of the heavy ion and depending on the target material, the heavy ion comes to a rest in the device after losing its energy (shallow strike) or the heavy ion traverses the entire device (deep strike). The total path travelled by the particle in the target material before it comes to a rest is called the range of the particle. The Linear Energy Transfer (LET) is the measure of the energy lost by the ion, which can be defined as the energy lost by the particle per unit path length as it passes through the target material. The most commonly used definition for LET is obtained by dividing the energy loss per unit by the material density (ρ):

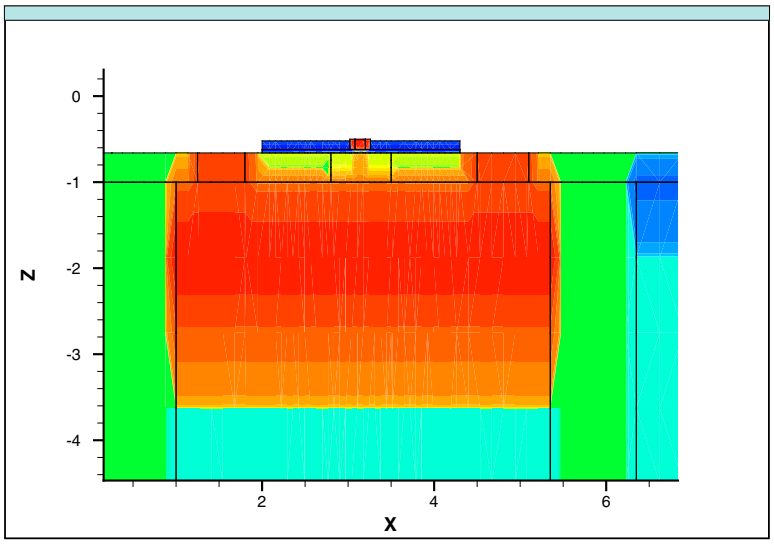


Figure 2.7: 2-D View of the 8HP regular HBT (cut made at the center of the emitter). Color indicates doping profile.

$$LET = \frac{1}{\rho} \times \frac{dE}{dX}$$

The LET defined above has a unit of MeV cm^2/mg. The LET of the ion can be related to the charge deposition per unit length because it takes a certain amount of energy to release carriers for a particular material. In silicon one electron-hole pair is released for every 3.6 eV energy released by the incident ion. The density of silicon is 2328 mg/cm^3. Hence an LET of 97 MeV cm^2/mg corresponds to a charge deposition of 1 pC/μm.

LET should be specified in pC/μm for SEU simulations. In DESSIS, a constant LET or a variable LET can be specified. A variable LET is specified by a list of LETs at various depths. Variable LET is used for the microbeam-simulation comparison. The LET profile (LET Vs Depth) was simulated using SRIM (The Stopping and Range of Ions in Matter) [14]. In SRIM the target details and ion details are specified. The target material details include the material, the density of the material and thickness of the target. The ion details contain the material, the energy of the ion and the angle of incidence. The result is given in eV/A$_\circ$. A matlab code was written to convert the unit from eV/A$_\circ$ to pC/μm. The conversion is done as follows:

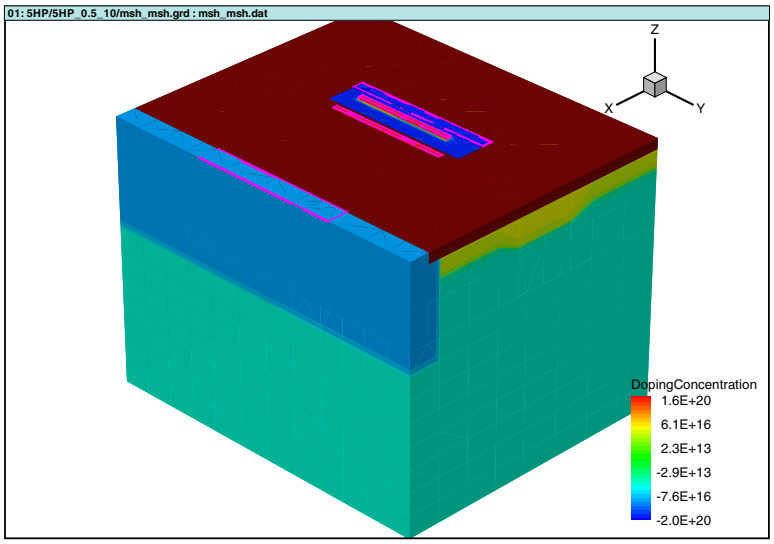


Figure 2.8: 3-D View of the 5HP regular HBT with emitter dimension 0.5 × 10 μm^2. Color indicates doping profile.

$$1\frac{eV}{A^\circ} = \frac{1\ eV}{3.6\ eV} \times 1.6 \times 10^{-19}\frac{C}{A^\circ}$$

A normal incident deep ion strike through the emitter with a uniform LET of 0.1 pC/μm (10 MeV-cm^2/mg) is simulated. This approximately corresponds to the LET of 36 MeV oxygen ion used in the microbeam test. The target material used in simulation is silicon. Fig. 2.11 shows the LET as a function of depth for oxygen ion with energy 36 MeV. The range of the ion in silicon is 25 μm, which can be seen from the figure. In actual devices, there is passivation and interconnection layer on top of the active device. The thickness of the passivation layer can be got from the Scanning Electron Microscope (SEM) image of the device. SEM image of cross section of a 0.25 μm SiGe BiCMOS is shown in Fig. 2.10. In SRIM, the target material thickness includes the thickness of the silicon substrate and the thickness of the passivation and interconnection layer. The energy lost in passivation and interconnection layer can be accounted for by ignoring the energy lost in the passivation layer in the LET profile and taking into account the energy lost in the silicon layer only.

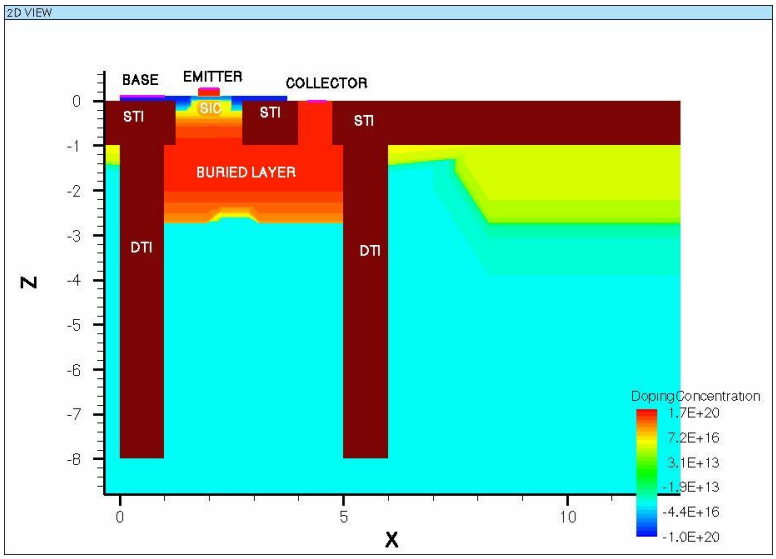


Figure 2.9: 2-D View of the 5HP regular HBT with cut at emitter center. Color indicates doping profile.

2.2.2 Charge Track Generation

When a heavy ion passes through the device it creates a trail of electron-hole pairs. These charges are collected by the electric field present in the device by drift and by diffusion. This collection of charges might give rise to heavy currents which can switch the logical state of a memory cell.

The point of strike is specified along with the direction of the ion track. In DESSIS [15], the generation rate due to heavy ion is computed by the following relation

$$G(l, w, t) = LET(l) \times R(w) \times T(t)$$

where l is the distance from the incident point and w distance from the track. T(t) is the gaussian function given by

$$T(t) = \frac{2\exp[-(\frac{t-t_0}{s_{hi}})^2]}{s.\sqrt{\Pi}[1 - erf(\frac{t_0}{s_{hi}})]}$$

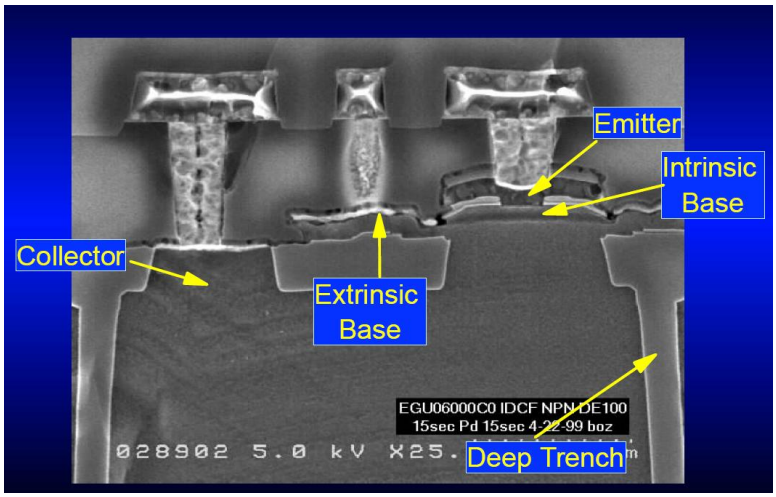


Figure 2.10: SEM image of cross section of 0.25 μm SiGe BiCMOS.

where t_0 is the time of ion-strike. s_{hi} is the characteristic value of the gaussian. LET(l) is given as a function of length. R(w) can be defined as either exponential or gaussian. In the exponential case

$$R(w) = \exp(-\frac{w}{w_i})$$

and for gaussian case

$$R(w) = \exp[-(\frac{w}{w_i})^2]$$

where w is radius defined as the perpendicular distance from the track. The characteristic distance w_i is defined in the input and can be a function of length [15].

A charge track containing a high density of electrons and holes is created when a heavy ion passes through the semiconductor material. This charge track is simulated in the simulation tool. The point of strike and the direction of strike is specified in the simulation. The simulation for the microbeam comparison is done for normal strike. The time of the ion strike is specified. The charge track was generated for a period of 10 picoseconds using a gaussian waveform. The 1/e characteristic time scale is 2 picoseconds and the 1/e characteristic radius is 0.1 μm. The peak of the gaussian occurs at 2 picoseconds. These constants are assumed to be independent of LET [16].

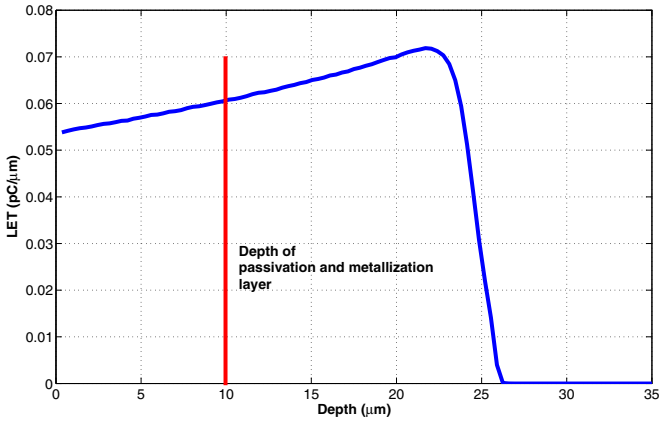


Figure 2.11: LET for oxygen with an energy of 36 MeV. The top 10 μm layer is the passivation and metallization layer, which is got from 8HP technology.

2.2.3 Meshing Strategy

The device has to be solved for the potential, electron and hole concentration [13]. In meshing, nodes are placed in the device and the equations are solved in each node. This might look easy but lot of intricacies go into meshing. Fine meshing should be placed at points where there is drastic changes of variables, like the pn junction. The charge track should have a lot of nodes because of the high density of charge in the track. If the ion strike is away from the CS junction, a fine mesh should be placed in the path between the junction and the ion track to account for the diffusion of charges towards the junction. The time taken for a simulation is proportional to N^{α}, where N is the number of nodes and α is a number between 1.6 and 2. Because of the exponential dependence, we have to optimize the node density to save time. Too coarse meshing gives inaccurate results. The average number of nodes used in the simulation are 12,000 to 17,000 which takes an average of 3 days for one complete transient simulation.

Fig. 2.12 gives the mesh in a 2D cross section for an ion strike at the center of the emitter. The mesh is fine immediately around the ion track and becomes coarser as the distance from the ion track increases. In the figure the mesh is very fine, which hides the intrinsic device.

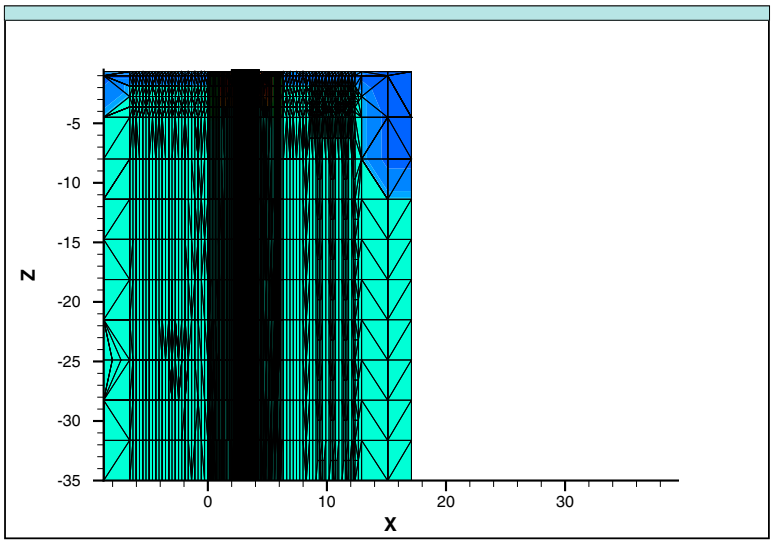


Figure 2.12: Meshing for an ion strike at the emitter center.

2.2.4 Numerical Issues

In addition to fine gridding along the ion path, the numerical discretization schemes are important for obtaining accurate charge collection simulation. In DEVISE, by default, the integration of the generation rate over the control volume associated with each vertex in the mesh is done with the assumption that generation rate is constant inside the vertex control volume and equal to generation rate value at the vertex. But heavy ion generation rates can change rapidly in space. Hence the approximation error with such an approximate approach may sometimes lead to very big errors. In particular this method does not guarantee charge conservation. To eliminate this source of numerical error an improved spatial integration is performed. Each control volume of the device is filled with small rectangular boxes and the generation rate is numerically integrated in these boxes [15].

2.2.5 Physical Models

The physical models selected in a simulation influence the accuracy of the result to a larger extent. So we have to be very careful in selecting the physical models. The most important models

selected in this simulation are Phillips unified mobility model, Auger recombination and bulk Schockley-Read-Hall (SRH) recombination and surface SRH recombination. The Phillips unified mobility model is used because it is more accurate for bipolar devices. Auger recombination is turned on when there is a heavy concentration of carriers. The velocity saturation parameter is also turned on.

Bulk SRH Recombination

Unwanted impurities in silicon lattice gives trap energy levels in the silicon bandgap. This trap acts as centers for electron-hole recombination. The bulk SRH recombination is important because of the high density of charges generated in the substrate of the device. The bulk SRH recombination rate is given by [15]

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)}$$

where

$$n_1 = n_{i,eff} \times \exp \frac{E_{trap}}{kT}$$

and

$$p_1 = n_{i,eff} \times \exp \frac{-E_{trap}}{kT}$$

where E_{trap} is the difference between the defect level and intrinsic level, n is the electron concentration and p is the hole concentration. $n_{i,eff}$ is the effective intrinsic carrier concentration.

$$n_{i,eff} = n_i \times \exp(\frac{\triangle G_{FD}}{2kT})$$

where ΔG is the change in bandgap due to heavy doping and germanium concentration. The default value of E_{trap} is zero which is used in all the simulations. The minority lifetimes τ_n and τ_p are modeled as a product of doping dependent, field dependent and temperature dependent factor. The doping dependence of SRH lifetimes is modeled with the Scharfetter relation

$$\tau_{dop}(N_i) = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + (\frac{N_i}{N_{ref}})^{\gamma}}$$

where τ_{min} has a default value of zero. τ_{max} has default values of 1×10^{-5} and 3×10^{-6} seconds for electrons and holes respectively. N_i is the doping concentration of the device and the reference doping concentration N_{ref} is 1×10^{16} cm^{-3} [15]. The τ_{max} and τ_{min} values are altered to fit the simulated data with the experimental data as will be seen later in this chapter.

Surface SRH Recombination

There are charge traps present in the silicon/oxide interface, which aids in recombination. IBM SiGe HBT device structure contains the Shallow trench and deep trench isolations, which are oxides. Hence the surface SRH recombination parameters are important for fitting of the microbeam and simulated data. The surface SRH recombination rate is given by

$$R^{SRH}_{surf,net} = \frac{np - n^2_{i,eff}}{\frac{(n+n_1)}{S_p} + \frac{(p+p_1)}{S_n}}$$

where S_n and S_p are the surface recombination velocities. They are given by the relation

$$s = s_0[1 + S_{ref}(\frac{N_i}{N_{ref}})^{\gamma}]$$

where N_i and N_{ref} are the same as the bulk SRH recombination parameters. S_{ref} is the doping dependent parameter of the surface recombination velocity, which has a default value of 1000. S_0 is the surface recombination velocity when the doping dependency is zero, which has a default value of 1000 cm/sec. The fitting parameters which are changed to fit the microbeam data with the simulated data are S_{ref} and S_0 [15]. The recombination velocity and the S_{ref} determine the recombination rates in the oxide/silicon interface. Their impact on surface recombination rate can be seen later in this chapter.

2.3 Terms in the World of SEU

This subsection gives important terms and their definitions used in the world of SEU [16].

- *Range*: The range R(E_0) is the projection of the "crow-flight" distance of the incident particle into the material in the direction of incidence. The range is roughly the penetration distance.

- *Critical Charge Q_C*: A threshold minimum or a critical LET that the incident particle should have to produce sufficient ionization -derived charge to cause an SEU within the sensitive node of the cell. This minimum charge is labeled as the critical charge. It is a function of the physical and electrical characteristics of the circuit in consideration. Q_C is the minimum charge incident at the memory storage node that causes a change of charge state - a bit flip. The concept of critical charge is important in digital circuits like flip-flops, memory circuits etc.

- *Funneling*: When a heavy high-energy ion penetrates a semiconductor device through its junctions and depletion layers, it produces a track of ionization, composed of electrons and holes from the semiconductor material atoms. The presence of the track temporarily collapses the depletion layers local to the track, distorting the equipotential surfaces of the depletion layer electric fields in the track vicinity. This distortion results in a nesting of funnel-shaped equipotential surfaces that can extend into the substrate bulk of the device. The funneling of the equipotentials produces a large potential gradient i.e. a large electric field in the funnel that propels the ionization electrons up the funnel in the SEU-sensitive node regions. There is a corresponding hole current directed down the funnel into the semiconductor substrate. There is a large increase in charge density collected, over that were there no funnel, thus increasing the probability that a critical charge is collected at a device information node.

  If the incident ion track passes very near the information node, most of the charge in the funnel is collected by the node depletion layers in fractions of nanoseconds following the track penetration. If the track lies remote from the node, the charge collection time is much longer, as the charge transport is principally by diffusion. After collection of the charge, the charge density falls to a level comparable to the substrate dopant density and the disturbed depletion layer field relaxes back to its state prior to the track onset.

- Cross Section: It is a probability coefficient that links the number of particle interactions of interest with the corresponding flux or fluence levels. It is the device SEE response to ionizing radiation. For an experimental test for a specific LET, σ = number of errors/(ion fluence). The units for cross section are cm^2 per device or per bit.

- Asymptotic Cross Section: The value that the cross section approaches as LET gets very large.

- LET Threshold: It is the minimum LET required to to cause a single Event Upset.

- Sensitive Volume: Sensitive volume refers to the device volume affected by SEE-inducing radiation. The geometry of the sensitive volume is not easily known, but some information is gained from test cross section data.

2.4 SEU Transient Current and Charge

The heavy ion generates a heavy charge density along its path in the target. The deposited charges are collected through drift and diffusion by the terminals of the device. The CS junction plays a major role in charge collection [17]. If the ion track passes through the junction electric field, the very high charge density generated by the ion collapses the junction field. Because of the shape of the perturbation it is termed as funnel. The funnel causes the junction field to penetrate deep into the substrate, below the original depletion region. Charges deposited deep in the substrate are collected by drift through the electric field in the funnel. The funnel depth depends on the substrate doping. The perturbation depth is large for a lightly doped substrate. Charges are collected by diffusion for ion tracks that does not pass through the junction. The substrate doping plays a major role in charge collection through diffusion. Higher the substrate doping lower the lifetime of the carriers, which leads to higher recombination rate in the substrate. So the charge collection reduces for higher substrate doping. In this section the charge collection mechanism for strikes inside DT and for strikes outside DT is shown.

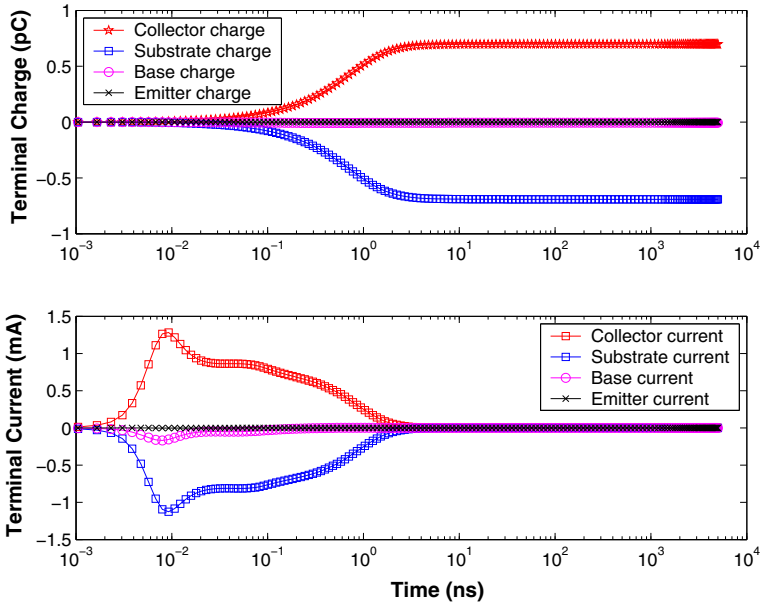


Figure 2.13: Terminal current/charge for an ion strike at emitter center for the 0.5 × 10 5HP HBT.

Fig. 2.13 shows the current and charge collection curve for a 0.5 × 10 5HP HBT for an ion strike at the emitter center. The heavy ion used is oxygen with an energy of 36 MeV and a variable LET is used. LET profile with depth is obtained from SRIM, which is shown in Fig. 2.11. The CS junction is reverse biased at -5.2 V. The charge curve is obtained by integrating the current curve. The charge collection starts by 0.05 ns and the collector and substrate collects most of the charges. The collector collects electrons and the substrate collects holes. The charge is collected through drift due to the perturbation of CS junction, which leads to funneling.

Fig. 2.14 shows the current and charge for a strike outside DT, 2.5 μm away from the outer DT edge. Unlike the emitter center strike, the charge collection starts at 3 ns. This is because the charges generated outside DT has to diffuse to the CS junction to be collected by the electric field in the junction. The diffusion of charges take more time and hence we see late charge collection. The charge curve saturates at 5 ns for the emitter center strike while it takes 300 ns for the outside DT strike.

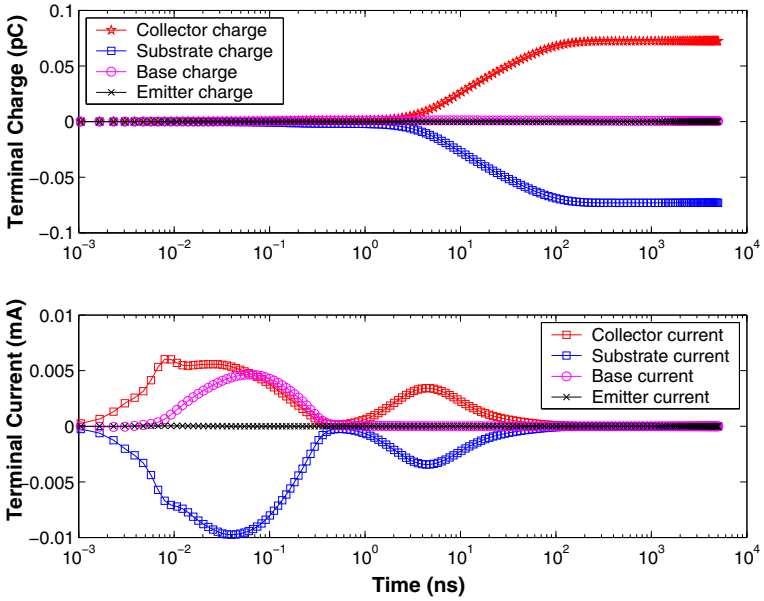


Figure 2.14: Terminal current/charge for an ion strike outside DT (2.5 μm away from outer DT edge) for the 0.5 × 10 5HP HBT. The ion used is 36 MeV oxygen with variable LET.

2.5 Microbeam Testing of HBTs

The major SEU inducing particles in microcircuit devices are cosmic ray heavy ions. Cosmic ray ions are the most energetic ions. Their charge consists of high multiples of the electron charge. The major source that simulate high energy cosmic ray ions that produce SEU are high-energy accelerators. The incident cosmic ray ions cause only soft errors through ionization interaction with the device material. The high energy accelerators used are mainly cyclotrons and Van de Graaf accelerators [16].

Sandia National Laboratory's Ion Beam Induced Charge Collection (IBICC) facility was used to study the charge collection characteristic in each terminal of the device and we were provided with the data obtained from the IBICC facility. A brief description of the experiment is given below. The die containing the devices is exposed to a chemical vapour etch process to remove polyimide that is on top of the die. After etching, the passivation layer contains several alternating metal/insulator and passivation layers. A four probe IBICC measurement is used to measure

simultaneously the charge collected by the collector (C), Emitter (E), Base (B) and Substrate (S) terminals due to a series of ion strikes occurring inside and outside the transistor area. Emitter, base and collector are grounded and the substrate is biased at -4 V. The flux is set sufficiently low to ensure that no more than one ion is incident on the die at each step [18].

The IBICC measurements were done using 36 MeV oxygen ions. The range of these ions in the silicon substrate is 24.5 μm. The thickness of the passivation layer(approximately 10 μm) is taken off from the range of the ion, to give the depth of penetration in the active device. The depth of the passivation layer was obtained from Scanning Electron Microscope (SEM) cross section image of the device. The ion beam spot size is 2 μm^2. The spot is stepped through a 1600 μm^2 area that contains the SiGe HBTs. The step size is 0.1 μm. The charges collected by the transistor terminals are obtained as a function of the location of the ion spot, i.e. the x and y coordinates. A measure of the accuracy of the IBICC measurement technique is to determine the net charge collected on all contacts and properly account for the sign of the charge. Holes are collected by the base and substrate and electrons are collected by the collector and the emitter.

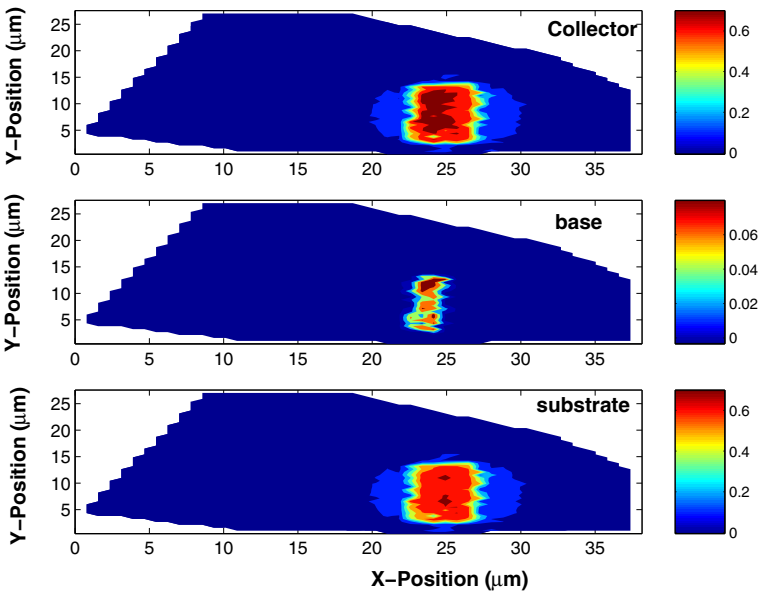


Figure 2.15: Contours of the charge collected by the collector, base and substrate as a function of the x and y coordinates of the ion strike location for 0.5 × 10 5HP device.

Fig. 2.15 shows the charge collection map obtained from the microbeam data for the 0.5 × 10 5HP device. The figure was obtained from matlab based on the results obtained from the microbeam experiment. Contours of the total charge collected by the collector, base and substrate are plotted versus the x and y coordinates of the ion strike location. The charge collection is maximum for collector and substrate over the area 5×13 μm^2 which is approximately the area of the CS junction.

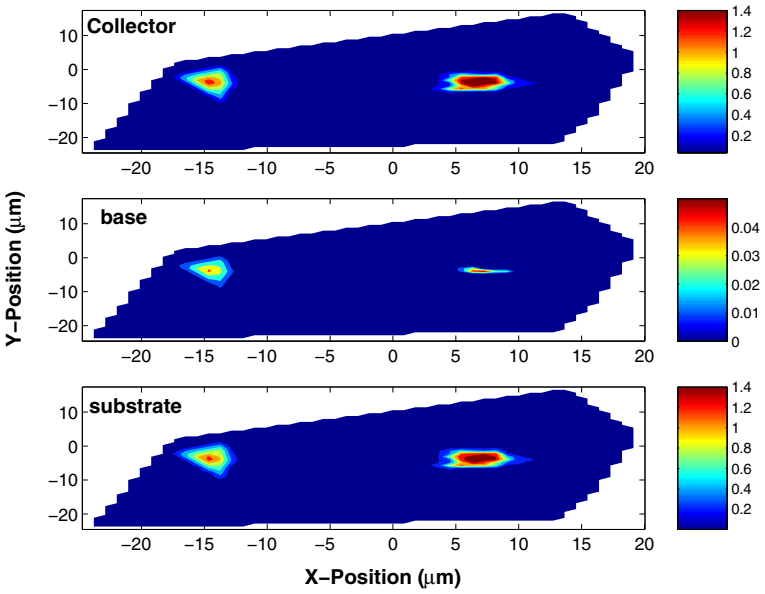


Figure 2.16: Contours of the charge collected by the collector, base and substrate as a function of the x and y coordinates of the ion strike location for 0.5 × 3 8HP device. The color variations at the left end of the figure is due to experimental errors.

Fig. 2.16 shows the charge collection map obtained from the microbeam data for the 0.5 × 3 8HP device. The charge collection is maximum for collector and substrate over the area 4.5×5 μm^2, which is approximately the area of the CS junction. The color variations at the left end of the device is due to experimental errors. The charge collected by the terminals depend on the area enclosed by the deep trench isolation. As we see from the above figures, the 5 HP device has a maximum charge collection in an area of 65 μm^2, which is the area enclosed by the deep trench in the 5 HP device.

2.6 Rectangular Parallelepiped (RPP) Model for Sensitive Volume

The chord distribution function plays an important part in the computational estimation of SEU or rate. Its importance stems as an outgrowth of the prototypical manner by which SEU and other interaction rates are computed classically: that is, in general, the sought after number of interactions of type x in a material volume induced by a penetrating particle flux ϕ is given by $\int N\sigma_x\phi dV$. σ_x is the cross section per flux particle per material "target" particle that characterizes the x interaction process. N is the number of material target particles per unit volume that will interact with ϕ in that way. In the case of SEU, there is a paucity of cross section functions σ by which an estimate of SEU error rate can be computed with the above integral.

Device immunity is determined by its LET threshold (LET_{th}), which is defined as the minimum LET to cause a single event effect at a particle fluence of 10^7 ions/cm^2. An elementary model of SEU behavior can be defined by using the concept of LET through some depth of a parallelepiped-shaped device. Fig. 2.17 shows a parallelepiped shape with dimensions a, b, and c, where c is the device depth. The energy deposited E_{dep} as the particle traverses a chord of length s through the sensitive volume of the device with density ρ is

$$E_{dep} = LET \times \rho \times s$$

The deposited charge (Q_{dep} depends on the energy required to generate an electron-hole pair, w_{ehp}.

$$Q_{dep} = \frac{E_{dep} \times q}{w_{ehp}}$$

where $q = 1.6022 \times 10^{-19}$ C. For silicon, the w_{ehp} is 3.6 eV. The minimum LET corresponds to the maximum chord length possible, s_{max}, which is the diagonal of the parallelepiped.

$$s_{max}^2 = a^2 + b^2 + c^2$$

The minimum LET necessary to cause an upset can be calculated from

$$LET_{th} = \frac{Q_{crit} \times w_{ehp}}{q \times \rho \times s_{max}}$$

Likewise there is a minimum distance, s_{min}, that a particle of given LET must travel before being able to deposit sufficient energy to cause an SEU.

$$s_{min} = \frac{Q_{crit} \times w_{ehp}}{q \times \rho \times LET}$$

The particle angle of incidence is also very important. As the angle of incidence increases from the normal to the device surface, the path length traversed by the heavy ion increases. The angle of incidence at which upset occurs for a given LET is known as the critical angle θ_c.

$$\cos\theta_c = \frac{LET}{LET_c}$$

. The particle that produce upset are between θ_c and $\pi/2$. We have to note that $LET_c < LET_{th}$. There are two potential cases:

- If $LET > LET_c$, then all incident angles produce upset.
- If $LET < LET_c$, then there is a critical angle θ_c, above which upset occurs.

Fig. 2.18 shows that particles incident at an angle θ travels $\frac{1}{\cos\theta}$ longer than the path at a normal incidence.

There are three basic steps in the calculation of SEU error rates:

- Measure the cross section versus LET using accelerator testing. The device cross section is the ratio of the number of upsets to the particle fluence.
- Determine the device sensitive volume. The sensitive volume is smaller than the actual device physical volume. The top area of the sensitive volume (σ_{seu}) is got from the asymptotic cross section in the cross section versus LET curves. The thickness of the sensitive volume is got from the range-energy relation written as

  $$c = R(E^{(o)}) - R(E^{(i)})$$

  where $R(E^{(i)})$ is the residual range after the particle at normal incidence has deposited energy E(c) in traversing through the sensitive region volume. Hence, the sensitive region volume can be estimated from $\sigma_{seu} \times c$.

- To determine the device error rate, integrate the cross section and sensitive device volume with the LET spectrum [19].

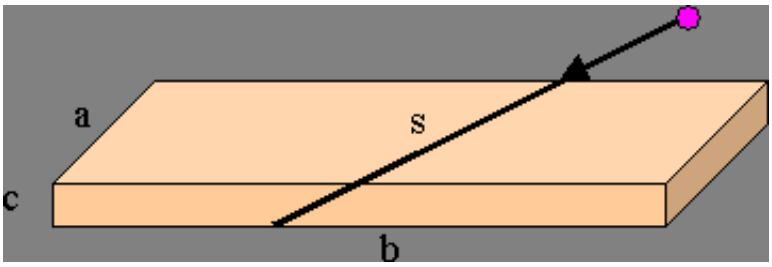


Figure 2.17: Parallelepiped shape with dimensions a, b, and c where c is the device depth.

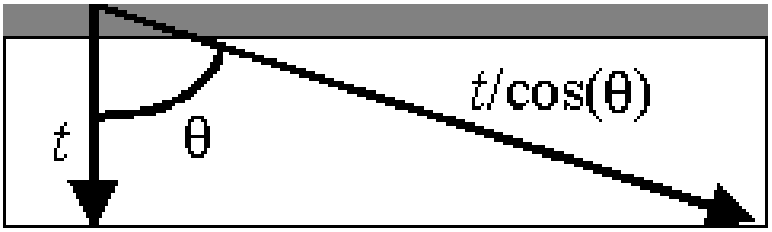


Figure 2.18: Particles incident at an angle θ have a longer path than the path at normal incidence.

Breakdowns in this model have been seen where the cross section is different for different particles that have the same effective LET. Traditional RPP models fail to spatially account for different charge collection mechanisms such as drift and diffusion. The RPP model tracks the charge deposited in a defined region but it fails to relate it to the charge collected in the sensitive circuit nodes. In SiGe HBTs the deep trench isolation truncates the charge collection by off normal ion strikes that cross the collector-substrate junction. Simulation and experimental data in SiGe HBTs suggests that the variation of the sensitive area is not typical of an RPP structure. The amount of charge collected is angularly dependent for particular LETs. With increasing angle in off normal strikes, the peak charge decreases but this lower peak charge is collected for a wider area [25]. Hence 3D simulation performed in this work helps in understanding and calculating SEU in SiGe HBTs.

2.7 Simulation/Microbeam Comparison

2.7.1 5HP HBT

The ion strike position is varied to find the dependance of charge collection by terminals on position. 3-D simulations are time consuming. So the simulation was performed in the critical portion of the device. The strike position is varied along the x-axis, with the y-coordinate is fixed at the center of the device. At each position, the strike simulated is a normal ion strike. From the contour plot of the microbeam test, we can identify the center of the device. Then the charge collection along the x-axis is plotted with the y-coordinate at the center. Then the emitter center of the microbeam device is aligned with the emitter center of the simulated device and the charge comparison compared.

The default parameters in DEVISE for the bulk SRH recombination and interface recombination does not give a good fit with the microbeam data. The doping dependence of the SRH lifetimes is modeled with the Scharfetter relation given by

$$\tau_{dop}(N_i) \;=\; \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + (\frac{N_i}{N_{ref}})^{\gamma}}$$

where the default value for τ_{min} is 0 for electrons and holes and default value for τ_{max} is 1×10^{-5} s for electrons and 3×10^{-6} for holes. The N_{ref} has a default value 1×10^{16} cm^{-3}. The default value of E_{trap} is used, which is zero. Hence the n1 and p1 values are $n_{i,eff}$. Now the formula for the bulk recombination rate becomes

$$R_{net}^{SRH} \;=\; \frac{np - n_{i,eff}^2}{\tau_p(n + n_{i,eff}) + \tau_n(p + n_{i,eff})}$$

Now the values of τ_n and τ_p depends on three important factors: doping dependent factor, temperature dependent factor and field dependent factor. The temperature and field dependent factor are constant in all our simulations. Hence the electron and hole lifetime can be written as

$$\tau_c \;=\; K \times \tau_{dop}$$

where K is the temperature and field dependent factor.

$$\tau_{dop} = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + (\frac{N_i}{N_{ref}})^{\gamma}}$$

τ_{min} has a default value of zero, which is used in all the simulations. Also $\gamma = 1$ and N_{ref} is $1 \times 10^{16}\ cm^{-3}$. Hence the formula reduces to

$$\tau_{dop} = \frac{\tau_{max}}{1 + \frac{N_i}{1 \times 10^{16}}}$$

. The highest doping is in the emitter which is in the range $1 \times 10^{21}\ cm^{-3}$ and the doping in the substrate is $1 \times 10^{15}\ cm^{-3}$. The sub-collector has a doping of $1 \times 10^{18}\ cm^{-3}$. But the higher doping regions are present only in the intrinsic part of the device and most of the device space contains the substrate doping. The τ_{dop} value ranges from τ_{max}/100001 in the emitter to τ_{max}/101 in the sub-collector to $10 \times \tau_{max}$ in the substrate. The sub-collector depth is approximately only 3 μm. Most of the ion track is in the substrate of the device. Thus changing τ_{max} gives a large variation in the charge collection, both for a strike event in the intrinsic and extrinsic part of the device.

DEVISE models doping dependence of surface recombination velocities as

$$s = s_0[1 + s_{ref}(\frac{N_i}{N_{ref}})^{\gamma}]$$

where the default values of s_0, s_{ref} and N_{ref} are 1000 cm/sec, 1000 and 1×10^{16} cm^{-3} respectively. With $\gamma = 1$ and $N_{ref} = 1 \times 10^{16}$ cm^{-3}

$$s = s_0[1 + s_{ref}(\frac{N_i}{1 \times 10^{16}})]$$

As explained in the previous paragraph, the doping varies in the intrinsic part of the device and almost constant in the substrate which occupies most part of the device. $\frac{N_i}{N_{ref}}$ varies from 10000 in the emitter to 100 in the sub-collector to 0.1 in the substrate. For a strike occurring at the center of the emitter, the ion track is surrounded by deep trench isolation, which has an large area of oxide/silicon interface. Also the doping varies extensively in the intrinsic part. But for a strike outside DTI, the silicon/oxide interface area is very less compared to the strike inside DT. Hence the surface SRH parameters are important for strikes inside DT.

The default bulk recombination parameters give the electrons and holes a long lifetime. The τ_{max} is changed to fit the microbeam data. The s_0 and s_{ref} are also changed to get the interface recombination for the particular device. The parameters explained in the above are varied to get a fit of the simulated data with the experimental data. For the 5HP device, a τ_{max} value of 47 ns and S_0 value of 600 cm/sec and the doping dependent parameter s_{ref} is switched off by changing it to 0. Fig. 2.19 shows the comparison between the microbeam and simulation result. There is a good

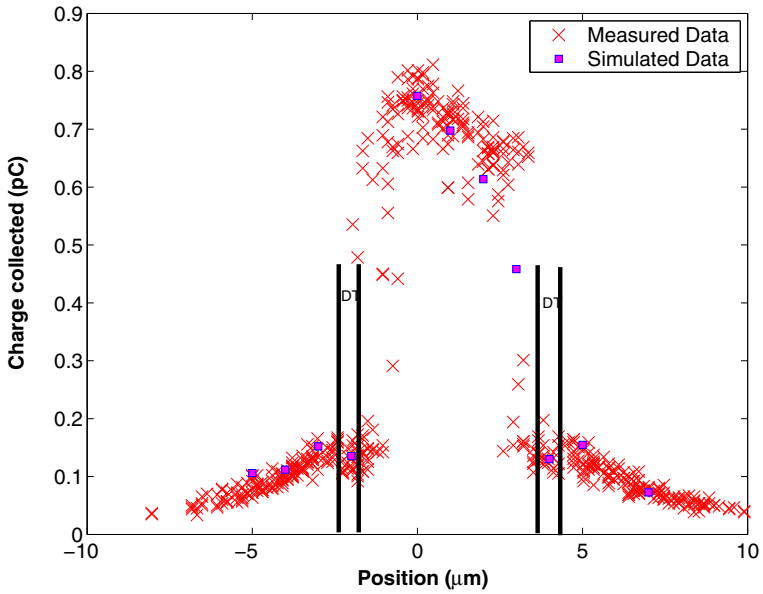


Figure 2.19: Microbeam/Simulation comparison for the 5HP 0.5x10 device. The ion-strike position is varied along the x-axis with the y-coordinate constant at the emitter center. τ_{max} = 47 ns, S_0 = 600 cm/sec, s_{ref} = 0

fit for strikes inside and outside DT. The parameters that change the bulk recombination rate is very important for strikes outside DT. The intrinsic device is surrounded by deep trench isolation, which is SiO_2. The recombination rate at the Si/SiO_2 is determined by the surface recombination parameters. The surface recombination parameters are important for strikes inside DT.

Fig. 2.11 shows the charge deposited in the device when a 36 MeV oxygen ion traverses the device. As explained before, the first 10 μm charge deposition is neglected to take into consideration the energy lost in the passivation and metallization layer. Fig. 2.13 shows the terminal current

and charge collection curves for the ion strike at the center of the silicon volume inside the DT region. We can see that initially the charge collection is through drift, which starts faster due to the funneling. Then we can see a different slope in the charge collection curve, which is slower than the initial drift collection. This collection is due to the diffusion of charges. The physics behind this can be given by the following explanation. Initially the ion track disturbs the subcollector junction, forming a funnel, which extends deep into the substrate. This funnel field collects charge through drift. Once the subcollector junction returns back to its original condition, the charge that remains in the substrate is collected through diffusion. The recombination parameters are important during the diffusive charge collection.

Initially the simulation was performed for two points. One simulation point is strike at the center of the emitter and the other point is strike outside DT. The bulk SRH parameters and the surface SRH parameters are tweaked to fit the experimental data with the simulated data for strikes at the emitter center and for strike outside DT. Once we get a good fit for the two points, the simulations are performed for more points in the device. This microbeam data comparison was performed for the 5HP 0.5×1.0 device. Fig. 2.20 shows the microbeam simulation comparison for

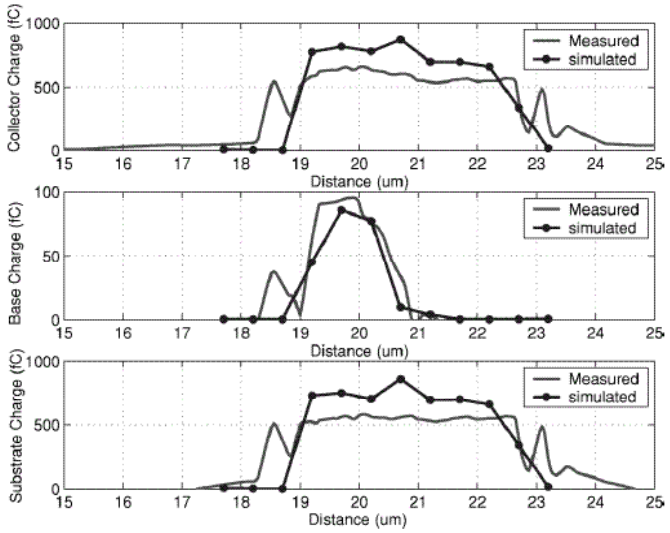


Figure 2.20: Microbeam/Simulation comparison for the 5HP 0.5x1.0 device. The ion-strike position is varied along the x-axis with the y-coordinate constant at the emitter center.

0.5×1.0 5HP device. The comparison is done for collector, base and substrate terminal. Although the fit between the microbeam and simulation data are not perfect, the simulation data follows the trend in the microbeam data. That is the charge collection is maximum for strikes inside DT and rolls off for strikes outside DT. A similar strategy is followed for the 8 HP device also.

2.7.2 8HP HBT Comparison

A similar fitting procedure as the 5HP was followed for the 8HP 0.12 × 3.00 device. The τ_{max} was varied for changing the bulk recombination rate and the s_0 and s_{ref} were changed for changing the interface recombination rate.

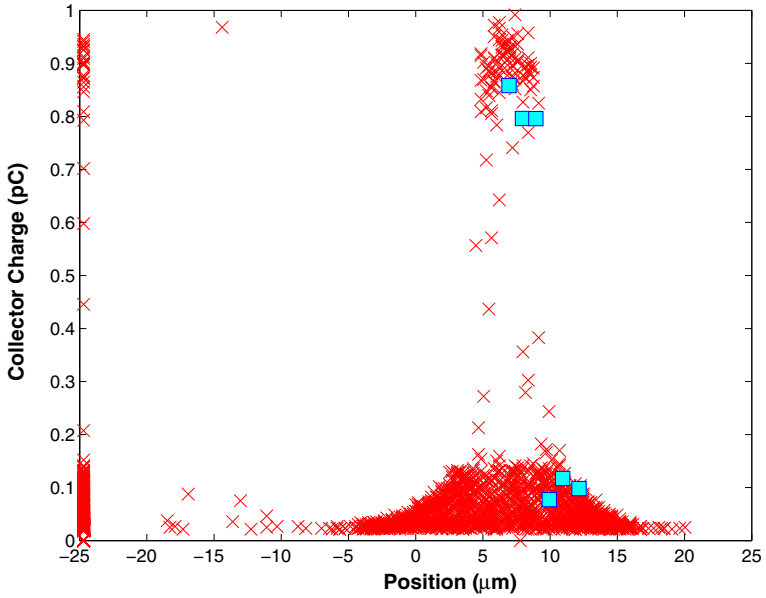


Figure 2.21: Microbeam/Simulation comparison for the 8HP device.

Fig. 2.21 compares the microbeam and simulation data for the 8HP 0.12 × 3.00 device. A τ_{max} value of 47 ns and S_0 value of 600 cm/sec and the doping dependent parameter $s_{ref} = 0$ gives a good fit outside DT but the fit is bad inside the DT. Hence, based on the strategy followed for the 8 HP structure, the surface SRH parameters are changed to get a good fit inside DT. The bulk and surface SRH parameters are changed to fit the simulated data. Each simulation takes 4 days to

complete. Hence only two points were done for various parameters: one at the center of emitter and the other 2 μm away from the outside edge of the DT. The impact of each parameter change was discussed in the previous section. Table 2.1 shows the simulated and microbeam charge

Table 2.1: Charge collection for strike at the emitter center.

$Q_{microbeam}$ (pC)	τ_{max} (ns)	S_{Ref}	S_0 (cm/sec)	$Q_{simulated}$ (pC)
0.9120	47	0	2000	1.4147
0.9120	20	0	3000	1.3390
0.9120	20	0	6000	1.3246
0.9120	20	0	30000	1.2277
0.9120	20	50	3000	1.2750
0.9120	65	0	600	1.5554
0.9120	65	1000	600	0.8983

comparison for different parameters for an ion strike at the emitter center. Table 2.2 shows the

Table 2.2: Charge collection for strike outside DT.

$Q_{microbeam}$ (pC)	τ_{max} (ns)	S_{Ref}	S_0 (cm/sec)	$Q_{simulated}$ (pC)
0.1100	47	0	2000	0.2087
0.1100	20	0	3000	0.1227
0.1100	20	0	6000	0.1176
0.1100	20	0	30000	0.0863
0.1100	20	50	3000	0.0992
0.1100	65	0	600	0.1693
0.1100	65	1000	600	0.01

simulated and microbeam charge comparison for different parameters for an ion strike outside DT. Changing τ_{max} affects the charge collection for strike inside and outside DT, as can be seen in both the tables. With $\tau_{max} = 20$ ns and $S_{ref} = 0$, changing s_0 from 3000 to 30000 cm/sec changes charge collection by 0.1113 pC for inside DT strike and 0.0364 cm/sec for outside DT strike. Hence we can see that changing s_0 by 10 times changes charge collection to a larger extent for strikes inside DT. With $\tau_{max} = 65$ ns and $s_0 = 600$ cm/sec, changing s_{ref} from 0 to 1000 changes charge collection by 0.6571 pC for strike at the emitter center and 0.1593 for a strike outside DT. Hence we can see that changing surface SRH parameters changes the charge collection for strikes inside DT by a large amount. This is true for both 8HP and 5HP. From the table, for the strike

at the emitter center, there is a good agreement between the microbeam and simulation for τ_{max} = 65 ns, S_{Ref} = 1000 and S_0 = 600 cm/sec. For the same parameter values the comparison between microbeam and simulation is way off for a strike outside DT. For the strike outside DT, there is a good agreement between the microbeam and simulation for τ_{max} = 20 ns, S_{Ref} = 0 and S_0 = 6000 cm/sec. For the same parameter values the comparison between microbeam and simulation is way off for a strike at the emitter center. Although the fitting for the 8HP is not good for strikes inside and outside DT, we can see that the simulated data follows the trend in the microbeam data. The charge collected is maximum for the strike at the emitter center in both the microbeam and simulated data and the charge collection decreases for strikes outside DT.

2.8 Charge collection comparison between 5HP and 8HP

The distance between the deep trench edges in 0.5×1.0 5HP is 6.20 μm whereas it is 6.0 μm for the 0.18×3.0 8HP device. Hence in the 8HP device, the DT is closer to the ion track than the 5HP device. Hence the surface SRH effect is more in the 8HP device than the 5HP device. From the above discussions, for default parameters in DEVISE and for an emitter center strike, the 8HP device collects 800 fC while the 5HP device collects 950 fC. Hence we can see that the surface SRH plays a major role in charge collection for strikes inside DT. As the device size decreases, the deep trenches come closer to the ion path. Hence there is more recombination at the silicon/oxide interface, which leads to less charge collection in smaller devices.

Thus we can see that the simulation data has a good fit for the 5HP 0.5×10 device. Although the fit is not good in 0.5×1.0 5HP and 0.18×3.0 8HP, it follows the trend as in the microbeam data. For strikes inside DT, the charges are collected through drift and diffusion and for strikes outside DT the charge collection mechanism is through diffusion.

Chapter 3

Charge Collection in SOI Devices

Collector-substrate junction plays a major role in charge collection. The normal method of hardening is to remove the collector-substrate junction. A natural approach to SEU hardening is to remove the p-type substrate, thus eliminating the n+ buried layer to p-substrate junction. In practice, this can be realized by fabricating the SiGe HBT on an SOI substrate, the feasibility of which has been demonstrated by various companies [20] [21] [22], primarily for reduction of parasitic capacitance and hence higher speed. In this chapter the collector-substrate junction is replaced with a buried oxide and the charge collection characteristic is studied for different N^+ buried layer thicknesses. The charge collection in SOI HBT is compared with the regular HBT [23].

3.1 Regular Device Charge Collection

In a regular device the collector and substrate terminal plays very important role in the heavy ion induced charge collection. The terminals collect charge by three mechanisms drift, diffusion and funneling. The ionized charges in the depletion region accelerates the mobile charges to be collected through the drift process. When the heavy ion path passes though a junction, it disturbs the potential in the junction. This disturbance goes deep into the substrate through a process called funneling. Funneling collect charges which are generated deep in the substrate through drift. Charges generated outside the depletion region and potential funnel are collected through diffusion.

Fig. 3.1 gives 2D cartoon view of the regular device. We can clearly see the emitter, base, collector and substrate contact.A cut at the center of the emitter gives Fig. 2.7, which is a 2D cross section of the device.

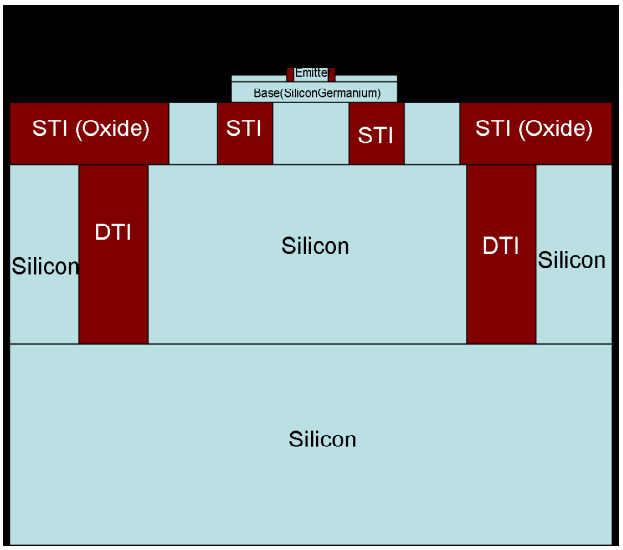


Figure 3.1: Schematic showing the different materials used in construction of device. 3d view of the regular device.

The ion used in the simulation was 1 GeV Fe ion. SRIM simulations showed an average LET of 12 $\frac{MeV-cm^2}{mg}$ which is equivalent to 0.1111 $\frac{pC}{\mu m}$. The ion traverses the entire device. The position of the ion strike is at the center of the emitter. All the terminals are grounded.

Fig. 3.2 and Fig. 3.3 gives the terminal currents and charges respectively for the strike at the center of emitter. Current entering the terminal are positive. The charge is obtained by integrating the terminal currents over time. Electron charge collection occurs primarily through the collector and emitter. Hole charge collection occurs through base and substrate. The ion path passes through the emitter-base, base-collector and collector-substrate junction. Hence we have drift and funneling mechanism in charge collection. The charges generated beyond the ion path are collected by diffusion. The different mechanisms of charge collection can be seen in a log plot.

Fig. 3.4 gives the log plot of the charge collection curve. We can clearly observe different regions of charge collection. As the ion strike is at the center of the emitter, the initial charge collection is through drift by funneling, which is shown by the initial charge collection in the collector. The initial drift collection of holes is by the base terminal. The perturbed depletion region snaps back to its original condition after sometime. Then the collection of charge is through

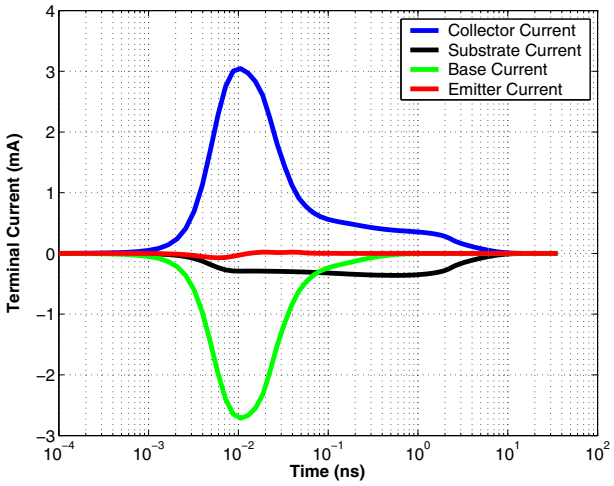


Figure 3.2: Terminal current for the bulk device.

the diffusion mechanism. We can see that the substrate terminal collects charge only through diffusion.

Fig. 3.5 gives the potential contour of the bulk device. The disturbance in the collector substrate junction potential goes deep into the substrate. The deep penetration of the potential perturbation into the substrate is primarily due to the light doping of the p-type substrate.

3.2 SOI Structure

The 0.5 μm bulk device is now simulated on an SOI structure. The SOI structure requires some process changes in fabrication. The n+/p/n emitter-base-collector layers are kept exactly the same for comparison with the bulk structure.

Fig. 3.6 shows the 3D view of the device. The color indicates the doping level. Fig. 3.7 shows a 2D cross section obtained from a cut through the center of the 3D structure. The device has a p-substrate with the same doping concentration as the bulk structure. There is a 0.4 μm thick buried oxide below the n+ layer. The active device is surrounded by trench isolation and buried oxide. The highlight of the SOI technology is the absence of collector-substrate junction, which played a major role in the collection of charge in the bulk device.

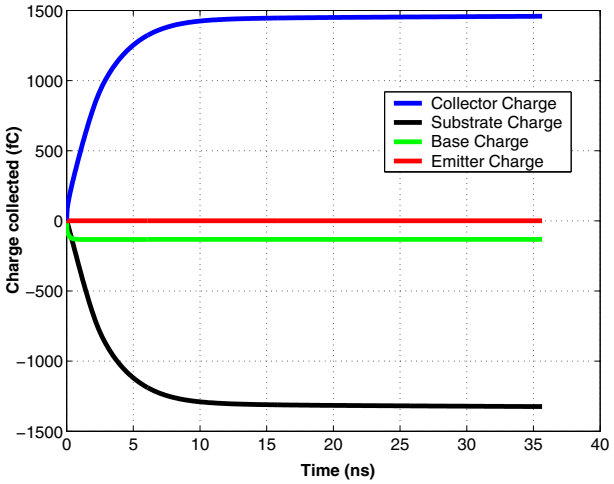


Figure 3.3: Terminal charge for the bulk device.

3.3 Charge Collection

In bulk device the collector-substrate junction plays an important role in the charge collection by the collector and the substrate terminals. In the SOI technology the collector-substrate junction is replaced by buried oxide. In Fig. 3.7 we see the thickness of the buried layer marked as t(n+). We have studied the charge collection for various n+ layer thickness.

3.3.1 Impact of n+ layer thickness

Naively one expects that the charge collection in SOI devices is proportional to the thickness of the insulator layer. The higher the thickness of the silicon on the insulator layer, higher is the charge deposited. The intrinsic n+/p/n layers corresponding to the emitter, base and collector set the minimum thickness of the silicon layer above the buried oxide. These layers are necessary to maintain the basic transistor functionality. Hence the only possible way to vary the silicon thickness is by varying the thickness of the n+ buried layer as shown by t(n+) in Fig. 3.7. A thinner n+ buried layer leads to increased collector resistance and increased saturation voltage which are undesirable. If a smaller thickness leads to significant reduction of charge collection, then a trade-off can be made between improving SEU immunity and reducing collector resistance.

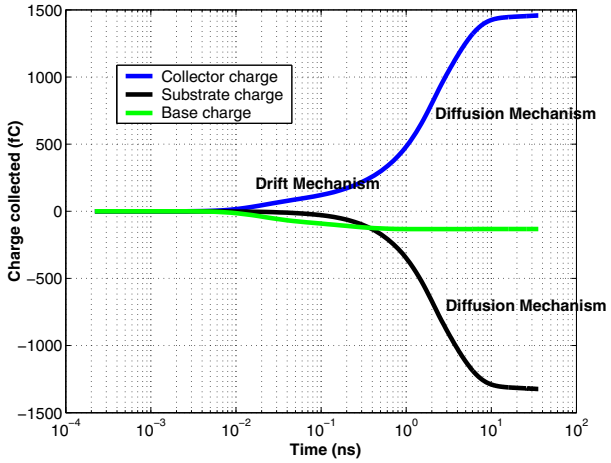


Figure 3.4: Terminal charge for the bulk device(log plot).

Fig. 3.8 shows the terminal currents simulated for five n+ layer thicknesses. The ion strikes were performed on the center of the silicon island, surrounded by the trench isolation. The terminal current transients are approximately the same for all the n+ layer thicknesses simulated. Fig. 3.9 shows the terminal charge collected for different n+ layer thicknesses. We can clearly see that the charges collected are independent of the n+ layer thickness. Substrate and emitter currents are negligibly small for all thicknesses as expected.

Table 3.1: Charge deposited and collected for different n^+ layer thicknesses.

n^+ thickness	$Q_{collected}$ (fC)				$Q_{deposited}$(fC)
	Q_{coll}	Q_{base}	Q_{emit}	Q_{subs}	
1.0 μm	133	-133.1	0.27	0.043	144.3
1.5 μm	133	-133	0.25	0.044	203.68
1.8 μm	133.4	-133.8	0.263	0.038	244.42
2.5 μm	136	-135.5	0.32	-0.66	311.08
3.0 μm	133.3	-133.5	0.272	-0.056	366.63

Electron charge collection occurs primarily through the collector and the hole charge collection occurs through the base. The substrate collects negligible charge. Table. 3.1 compares the charge deposited in the active volume above the buried oxide against the charges collected by various terminals. In the 1 μm thick n+ layer HBT 144.3 fC of charge is deposited in the SOI film. The

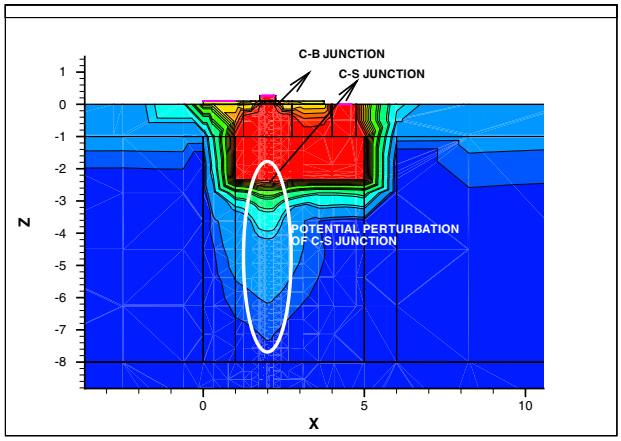


Figure 3.5: Potential contours in the bulk.

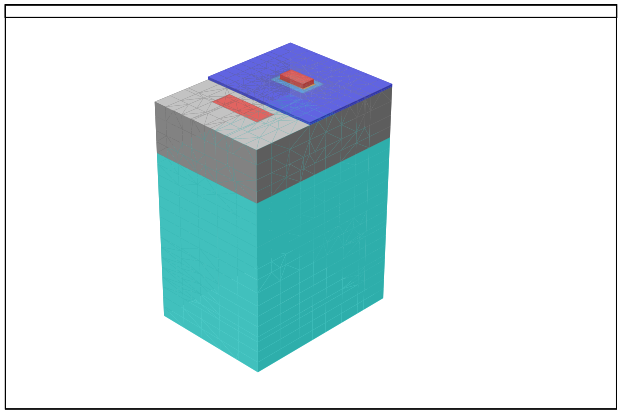


Figure 3.6: 3D view of the device. Color indicates the doping level.

charges collected by the collector and base are 133 and -133.1 fC respectively. A negative charge indicates that positive charges flow out of the base terminal. The charge deposited increases from 144.3 fC for 1 μm thick n+ layer to 366.3 fC for a 3 μm thick n+ layer. However the charges collected by the collector and base are approximately independent of the n+ layer thickness. The emitter charge collection is negligibly small compared to the collector and base charge collections.

The weak dependence of charge collection on n^+ layer thickness is attributed to the heavy doping of the n^+ layer. The passage of the ion causes an electrical field perturbation in the collector-base junction, or funneling of the potential distribution. Owing to the heavy doping of the n^+ layer,

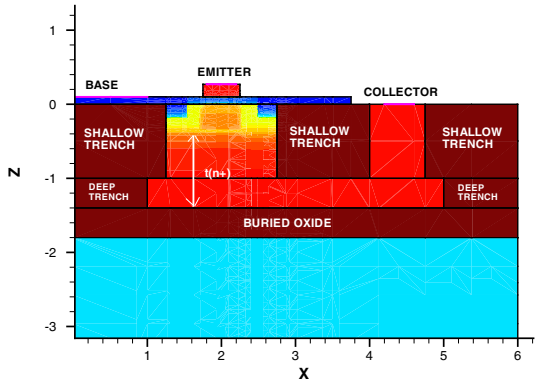


Figure 3.7: 2D cross section of the SOI SiGe HBT simulated.

the funnel does not penetrate deep into the n^+ layer. As a result, charge collection occurs primarily above the n^+ layer, leading to the weak dependence of charge collection on n^+ layer thickness. Fig. 3.10 and Fig. 3.11 show the simulated electrostatic potential contours at 9 ps for the $t(n^+)$ = 1 μm and $t(n^+)$ = 3 μm devices, respectively. The top portions of the HBT are zoomed to better visualize the potential perturbation in the collector-base junction. The buried oxide cannot be seen in Fig. 3.11 because of the thickness of the n^+ buried layer. The perturbation of potential for the $t(n^+)$ = 1 μm and = 3 μm HBTs are approximately the same. In both cases, the perturbation is confined within 0.1 μm above and 0.8 μm below the collector-base junction interface. To a large extent, this potential perturbation determines the amount of charge collection through drift. The nearly identical perturbation of potential for two devices with different n^+ layer thickness is responsible for the independence of charge collection on the n^+ layer thickness.

Assuming that all of the charges deposited within the potential funnel are collected through drift, a first order estimation of the charge collected can be made by calculating the product of the LET and the length of the potential funnel [24]. In this case, the lengths of the potential funnels are 0.9 μm according to the simulated potential distributions (Fig. 3.10 and Fig. 3.11). With an LET of 0.1111 pC/μm, the estimated amount of charge collection is 135.2 fC. This is quite close to the simulated numbers shown in Table I, which is from 133 to 136 fC for different n^+ thicknesses.

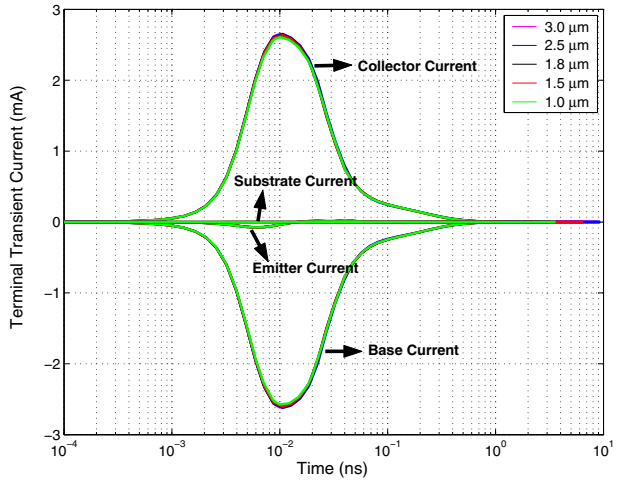


Figure 3.8: Transient current for 5 different thicknesses of the n+ layer.

3.3.2 Load Dependance

The SiGe HBTs are used in analog and digital circuits with various loads. To examine the impact of load on charge collection, simulations are performed with resistive and capacitive loads. The simulations are performed on the 1 μm thick n+ layer structure with different loads. The collector terminal is loaded with a Resistor R_L in parallel with a capacitor C_L of 1 pF. Resistor values of 0, 1 kΩ and 2 kΩ are simulated.

Table 3.2: Charge collection for different loads on collector.

	$Q_{collector}$	Q_{base}	$Q_{emitter}$	$Q_{substrate}$
No Load	133 fC	-133 fC	0.27 fC	0.042 fC
1 kΩ Load	123 fC	-129 fC	5.8 fC	0.031 fC
2 kΩ Load	114 fC	-127 fC	13 fC	0.048 fC

Figs. 3.12 and 3.13 show the resulting charge collection for the collector and emitter, respectively. The charge collected by the collector decreases with increasing R_L. The charge collected by the emitter, however, increases with increasing R_L. This load dependence is similar to that in bulk SiGe HBTs. The sum of the collector and emitter charges decreases slightly with increasing R_L. The increase of R_L also increases the time of charge collection, as can be seen from Figs. 3.12

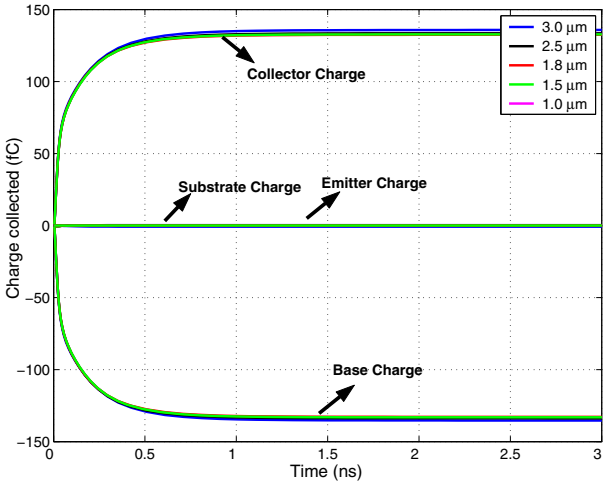


Figure 3.9: Terminal charge for 5 different thicknesses of the n+ layer.

and 3.13. Figs. 3.14 show the resulting charge collection for the base. Table 3.2 summarizes the charges collected by the terminals for different R_L.

The electrons deposited can exit the device through the collector and emitter. An increase in the load on the collector directs more electrons towards the least resistive emitter. Hence the charge collected by emitter increases with increasing R_L. With increasing R_L, exit of charges from the device is more difficult, leading to a longer charge collection time and more carrier recombination. Increased recombination leads to a decrease of the total charge collection with increasing R_L.

3.3.3 Bias Effect

One may expect that the charge collection depends on the terminal biases, the collector-base junction bias V_{CB} in particular, as the depletion layer width of the CB junction is much wider than that of the EB junction. For transistor in the data path of a D-flip flop, V_{CB} switches from 0 V to 0.3 V. For transistors in the clock circuit, V_{CB} is about 400 mV. The highest V_{CB} is about 2 V, found in the current mirrors. Fig. 3.15 compares charge collection for V_{CB}=0, 0.3 and 2 V. The base collects approximately the same amount of charge for all of the three biases. The charge collected by the collector is 20 fC higher at V_{CB}=2 V than at V_{CB}=0 and 0.3 V. Similarly, the

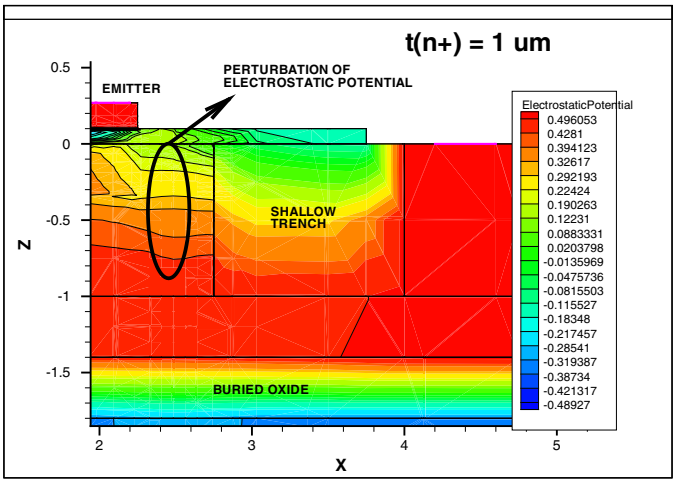


Figure 3.10: Electrostatic potential contours at 9 ps, for t(n^+) = 1 μm.

charge collected by the emitter is 20 fC higher at V_{CB}=2V than at V_{CB}=0 and 0.3 V. There is not a lot of difference in charge collection for various biases. The fact that the base charge collection remains independent of V_{CB} while both collector and emitter charge collections increase with V_{CB} by the same amount suggests that the primary role of a higher V_{CB} is to enhance the "short" circuit drift charge collection between emitter and collector, through a higher field between collector and emitter. The charge collection through the CB junction funnel is fairly independent of V_{CB}, primarily due to the heavy doping of the n^+ buried layer. The depletion layer width is primarily determined by the collector layer thickness.

3.4 SOI/Bulk Comparison

A logical question is how the charge collection characteristics in SOI HBT compare to those in a bulk HBT. To answer this question, we repeated the same simulation on the bulk counterpart of the SOI SiGe HBT discussed above. The substrate is grounded here, which represents the best case, as in circuits the substrate is always tied to the most negative potential, e.g. -5.2 V. In a bulk device, charge collection depends on the range of ion [1]. In this case, the range of the 1 GeV

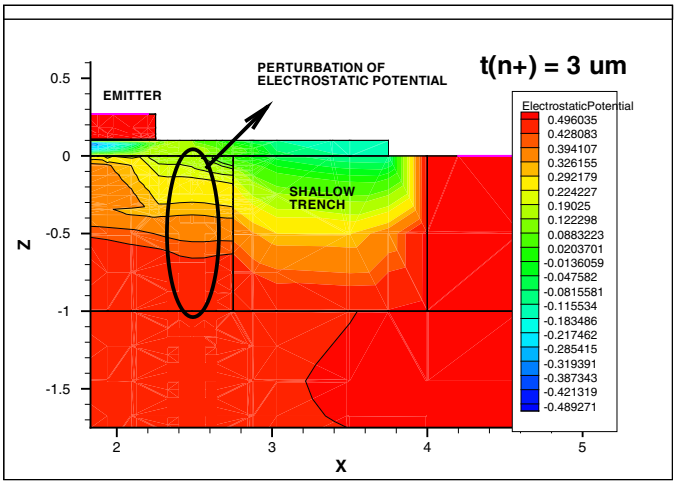


Figure 3.11: Electrostatic potential contours at 9 ps, for t(n^+) = 3 μm.

Fe ion is several hundred microns. In our simulation, only the first 25 μm of the bulk device is simulated due to simulator constraints. This is not exact, but should be sufficient for our purpose.

3.4.1 Collector/substrate comparision

Fig. 3.16 shows the terminal currents for the bulk and SOI SiGe HBTs up to 10 ns. For the SOI HBT, the transient collector current decays to zero at 1 ns. For the bulk HBT, the collector current decays to zero at 9 ns. The substrate current is negligible in the SOI HBT at all times due to the absence of collector-substrate junction. For the bulk HBT, the substrate current decays to zero at 9 ns.

Fig. 3.17 compares the bulk and SOI terminal charge collection characteristics up to 15 ns. The charge collection is complete in 0.8 ns in the SOI HBT while the charge collection is complete in 10 ns in the bulk HBT. The charge collected in the bulk HBT is 10 times the charge collected in the SOI HBT. For the SOI HBT, the substrate charge collection is negligible. For the bulk HBT, substrate charge collection is appreciable and comparable to the collector charge collection.

Fig. 3.5 shows the potential contours in the bulk HBT at 7 ps. The disturbance in the collector-substrate junction potential goes deep into the substrate which is why the collector charge collection is much higher in the bulk HBT than in the SOI HBT. The deep penetration of the potential

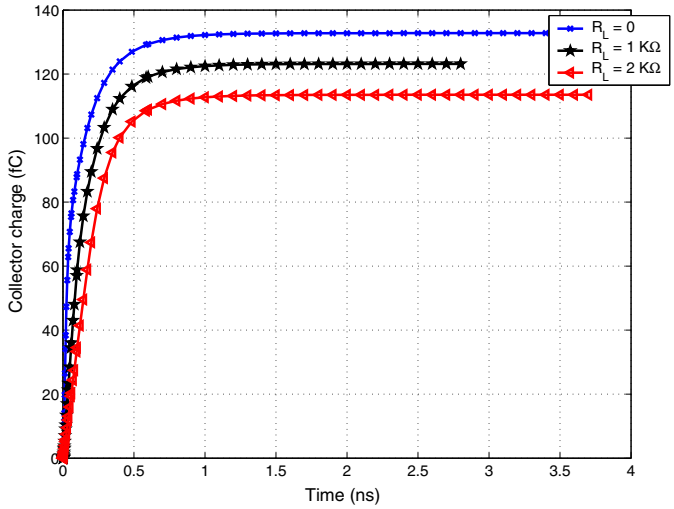


Figure 3.12: Charges collected by collector terminal as a function of load resistor.

perturbation into the substrate is primarily due to the light doping of the p-type substrate. For the same reason, charge collection takes a much longer time in the bulk HBT than in the SOI HBT. In bulk HBT, electrons are collected by the collector and holes are collected by the substrate, through the perturbation of the potential in the collector-substrate junction. On the contrary, in SOI HBT, the substrate collects negligible charge due to the removal of collector-substrate junction. If collector is the sensitive node, SOI HBTs offer significant advantage over bulk HBTs.

3.4.2 Base/emitter comparision

Interestingly, the base and emitter currents are virtually the same for the SOI and bulk SiGe HBTs. The base and emitter charge collection are about the same for the bulk and SOI SiGe HBTs. Base charge collection is complete within 0.8 ns in both bulk and SOI HBT and emitter charge collection is complete within 0.1 ns in both bulk and SOI HBT.

The reason for the similar base and emitter charge collection characteristics in the bulk and SOI HBTs is the decoupling of the charge collection in the active n^+/p/n emitter-base-collector layers from the charge collection in the n^+ buried layer to p-substrate junction. Fig. 3.5 shows the potential perturbation in the collector-substrate junction and collector-base junction. The potential

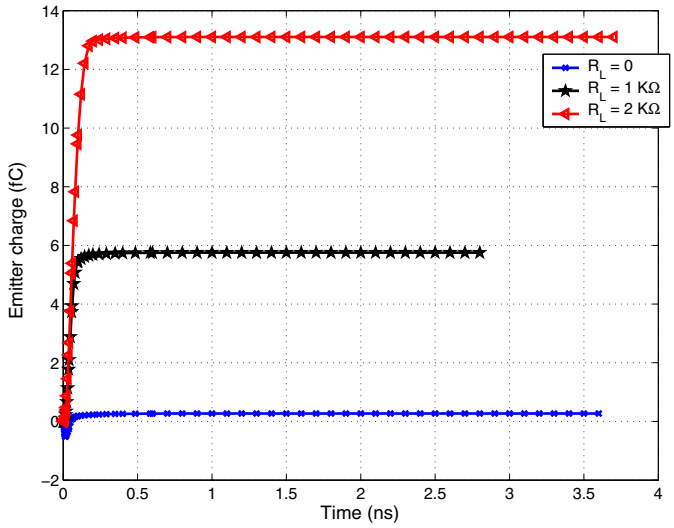


Figure 3.13: Charges collected by emitter terminal as a function of load resistor.

perturbation of the collector-base junction is confined within 0.8 μm below the collector-base junction. An undisturbed n^+ buried layer is sandwiched between the collector-base junction and the collector-substrate junction. The potential perturbation in the collector-base junction is essentially decoupled from the potential perturbation in the collector-substrate junction. This decoupling is physically enabled by the heavy doping of the n^+ buried layer. The potential perturbation in the active n^+/p/n emitter, base, and collector layers in the bulk and SOI HBTs are identical, as confirmed by the simulation details. As a result, the emitter and base charge collection characteristics are about the same in the bulk and SOI HBTs. If the base and emitter are the sensitive nodes of the circuit, SOI HBT offers no advantage over bulk HBT in terms of charge collection.

3.5 Conclusion

We have presented 3-D simulation of heavy ion induced charge collection in SiGe HBTs on SOI. The charge collection is found to take place above the n^+ buried layer. As a result, thinning the n^+ buried layer does not help reducing the charge collection. The load dependence of the charge collection is found to be similar to that for bulk HBT. Comparison with bulk HBT shows

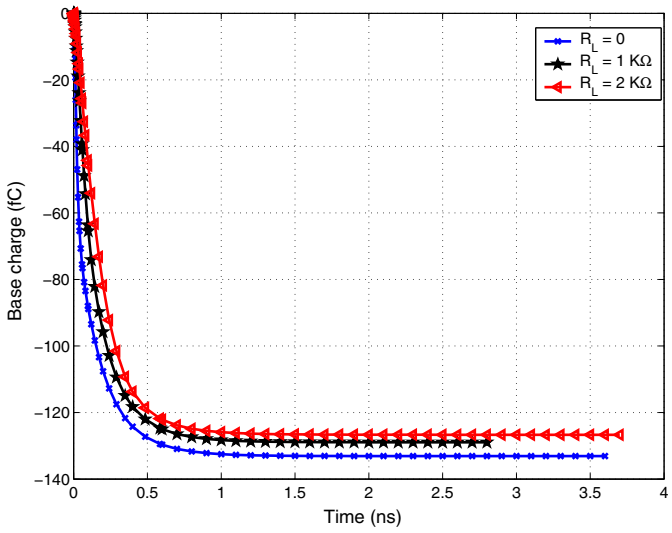


Figure 3.14: Charges collected by base terminal as a function of load resistor.

that the emitter and base charge collection characteristics are similar in bulk and SOI HBTs, due to decoupling of the charge collection in the $n^+/n/p$ intrinsic device and the charge collection in the n^+/p collector to substrate junction. SiGe HBT on SOI is effective in reducing the collector charge collection, thanks to the removal of the n^+ buried layer to p-substrate junction, as well as the heavy doping of the n^+ buried layer.

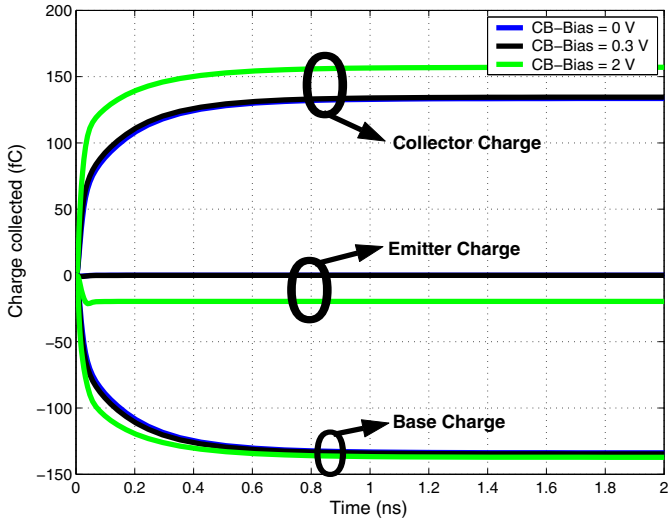


Figure 3.15: Charges collected as a function of time for different V_{CB}.

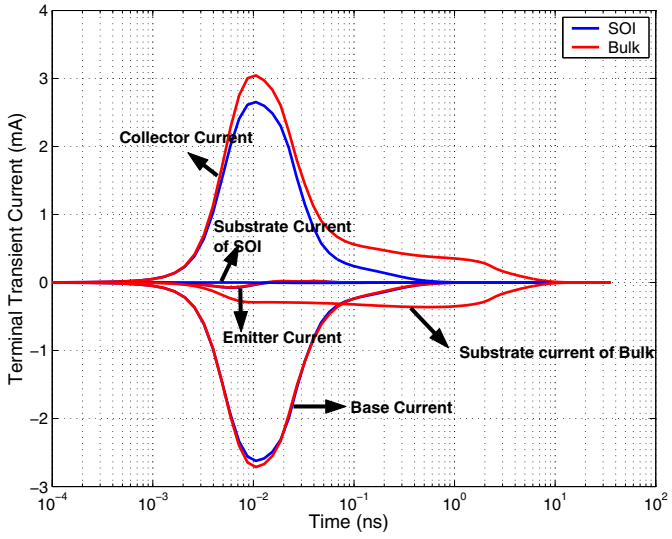


Figure 3.16: Comparison of terminal transient currents between bulk and SOI devices.

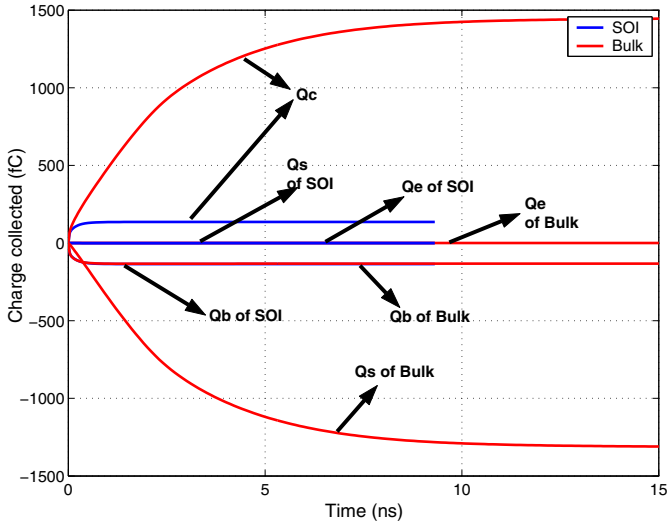


Figure 3.17: Comparison of terminal charge collection between bulk and SOI devices.

Chapter 4

Charge collection in Regular HBTs for normal and angled strikes

Heavy ions in space strike terrestrial electronic circuits in all possible angles. Large angled strikes are of more concern because more than 60 percentage of the strikes are large angled [26] [27]. This chapter examines the charge collection for normal and angled strikes in a regular 8HP HBT. Then the charge collection is studied for a 2×2 and 3×3 HBT array.

4.1 Simulation Conditions

An LET of 0.1 pC/μm, equivalent to 9.7 MeV cm^2/mg is used in all the simulations. The strike is a deep strike in which the ion traverses the entire device. As the ion passes through the entire device, it generates electron-hole pairs along its track. 3-D simulations are time consuming. So only specific points were simulated. The ion strike location was varied along the x-coordinate with y-coordinate constant at the center of the emitter. Fig. 4.1 shows the ion strike locations. The y-coordinate is at the center of the emitter and the x-coordinate is varied. The physical models used in the simulation are the same as in the chapter microbeam-simulation comparison. Default SRH recombination model parameters are used. The default parameters give longer lifetime of 9 μs for a substrate doping of 1×10^{15} cm^{-3}. This represents the worst case. Collector, emitter and base are grounded. Substrate is biased at -4 V.

4.2 Positional Dependence of Charge Collection

Simulations are performed at locations as shown in Fig. 4.1 at angles $\theta = 0°$, 30°, 45° and 60°. θ represents the angle of the ion track to the normal to the device surface. Fig. 4.2 shows collector charge versus ion incident position for various incident angles in the regular HBTs. We

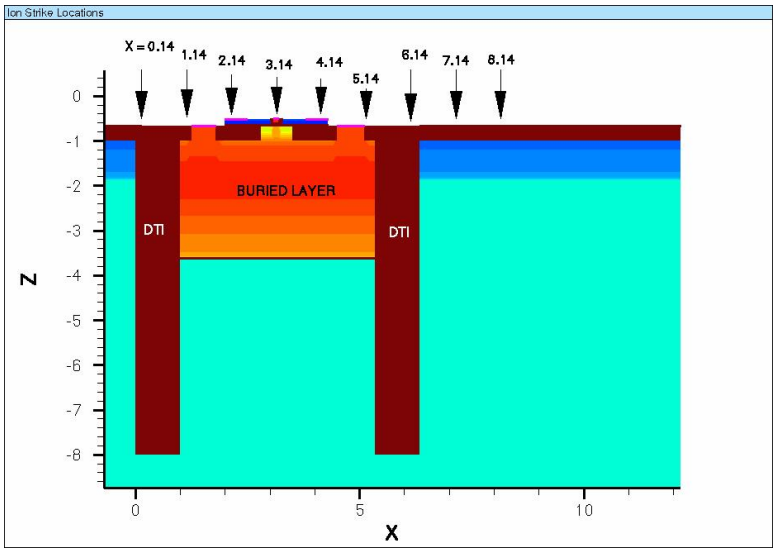


Figure 4.1: 2-D cross section of 8HP HBT showing ion strike locations. Cross section made at the emitter center. Color indicates doping.

are concerned about the collector terminal because collector is the sensitive node in most of the circuits. The figure clearly shows that the worst charge collection occurs for normal strike. As the angle of incidence increases inside DT, the charge collected decreases. This is because charge gets deposited outside the deep trench perimeter for angled strikes. As the angle of incidence increases, the area of maximum charge collection decreases. The collector collects large amount of charge even for strikes occurring outside DT because of the long lifetimes and large diffusion lengths.

The RPP model discussed in chapter 2 breaks down for angled strike in SiGe HBTs. Traditional RPP models fail to spatially account for different charge collection mechanisms such as drift and diffusion. In angled strikes, the charge track might miss the CS junction but still pass through the intrinsic device. The track lies in the sub-collector region and exits without disturbing the CS junction. There is no instantaneous drift charge collection. The RPP model tracks the charge deposited in a defined region but it fails to relate it to the charge collected in the sensitive circuit nodes [25].

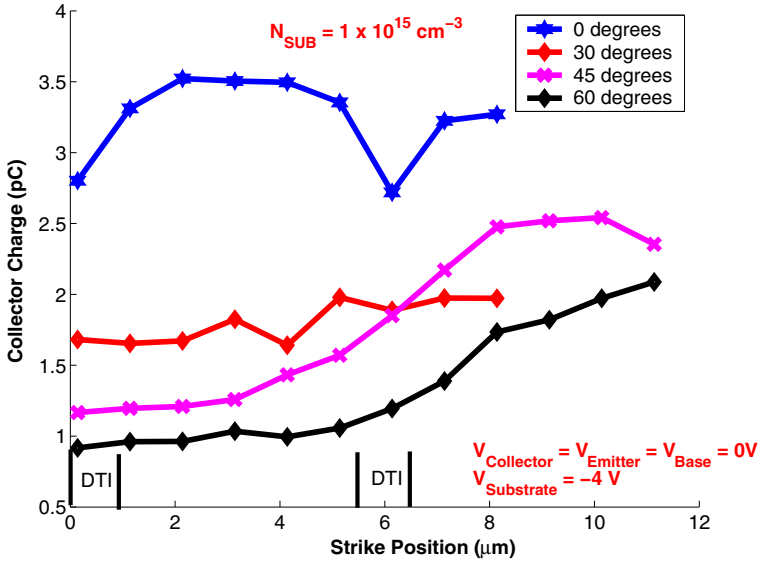


Figure 4.2: Collector charge versus strike location for incident angles $\theta = 0°$, $30°$, $45°$ and $60°$.

4.2.1 Terminal current and Terminal Charge collection

Charge collection is compared between normal and angled strike for emitter center strike and outside DT strike.

Emitter Center Strike

Terminal current and charge is compared for a strike at the emitter center inside DT. Fig. 4.3 shows the charge collection comparison between the normal and angled ion strike at the emitter center. The ion track for the normal strike passes through the CS junction of the device. So we have a funneling of the junction field, which leads to a heavy drift collection. Once the junction snaps back to its original state, charges start to diffuse collected by the field in CS junction. For the 30 ° strike, the ion track grazes the CS junction and hence we cannot see a heavy drift as in normal strike. Charges deposited outside the DT are collected through diffusion. For 45 ° and 60 ° strike the ion does not disturb the CS junction, which leads to late charge collection through diffusion.

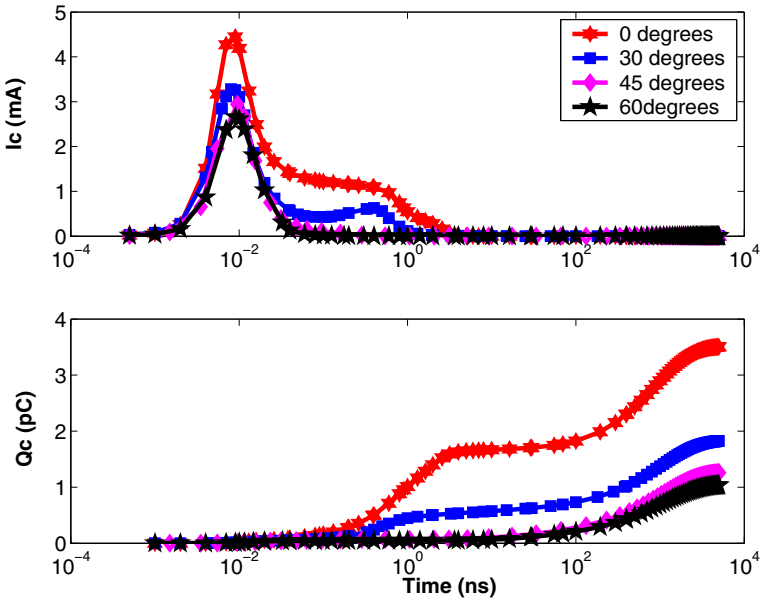


Figure 4.3: Terminal current and charge comparison for a strike at the emitter center (Inside DT).

Outside DT Strike

Terminal current and charge is compared for a strike outside DT, 2 μm away from the outer DT edge. Fig. 4.4 shows the charge collection comparison between the normal and angled ion strike occurring outside DT. The ion track in the normal strike does not disturb the CS junction, which leads to charge collection only through diffusion. For 30 ° and 45 °, the track passes through the collector-substrate junction, which leads to heavy drift initially and then through diffusion because of the longer lifetime. For 60 °, the ion track just grazes the CS junction, which leads to a light drift and then through diffusion.

4.2.2 Contours for Normal Strike

The charge collection and the funneling can be well understood with the snap shot of the device taken at various time instants in the transient simulation.

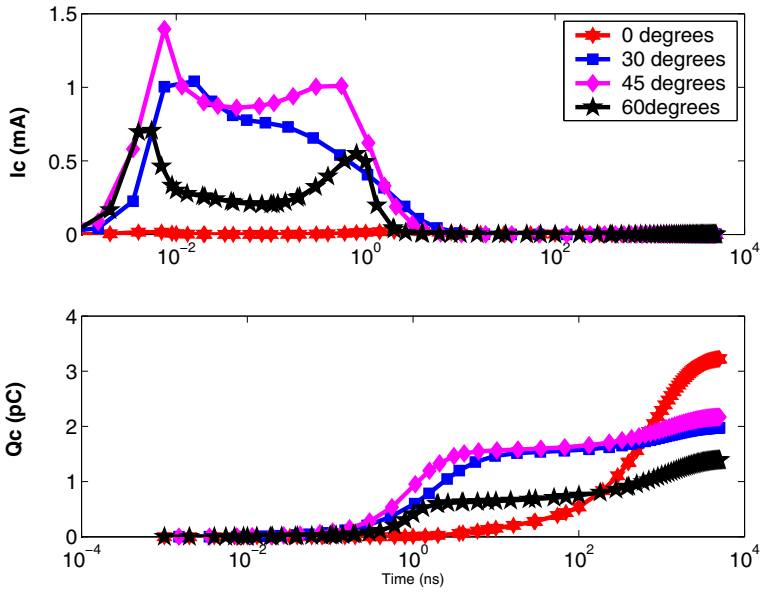


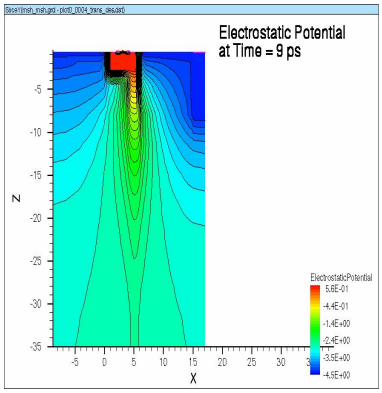
Figure 4.4: Terminal current and charge comparison for a strike outside DT.

Electrostatic Potential

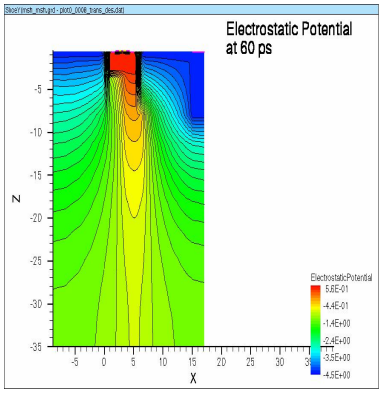
Fig. 4.5 and Fig. 4.6 shows cross section of the electrostatic potential at 9 ps, 60 ps, 800 ps and 4000 ps for a strike at the NS edge. We can clearly observe that the funneling of the potential in the CS junction. At 60 ps the intensity of the electrostatic potential inside the funnel decreases. At 800 ps we can clearly see that the funneling has reduced and the CS junction is returning back to its original state. At 4000 ps we can see that the CS junction is back to its original state.

Electron Density

Fig. 4.7 and Fig. 4.8 shows cross section of the electron density at 9 ps, 60 ps, 800 ps and 4000 ps for a strike at the NS edge. At 9 ps we can observe that the electron density track is confined in the funnel, getting collected through drift in the funnel. Even at 60 ps there is negligible diffusion due to the existence of the funnel. At 800 ps the funnel is coming back to its original state and the electron density has diffused outward. But the track is still present. At 4000 ps the track has extinguished and the diffusion is the only way of collection.

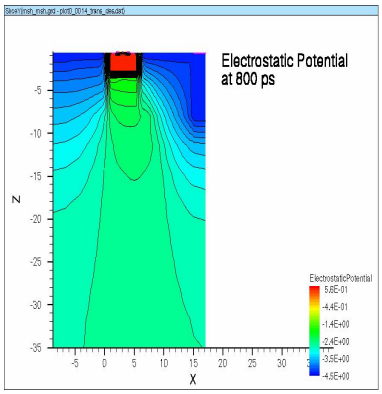


(a) t = 9 ps

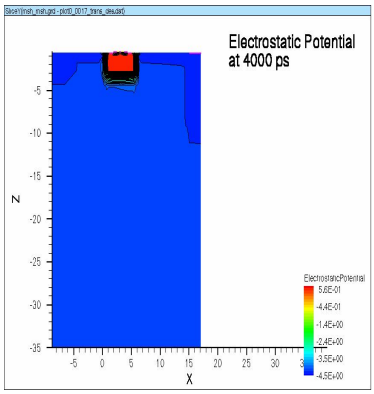


(b) t = 60 ps

Figure 4.5: Cross section of the device showing the electrostatic potential at 9 and 60 ps for a strike at x = 5.14 μm.



(a) t = 800 ps



(b) t = 4000 ps

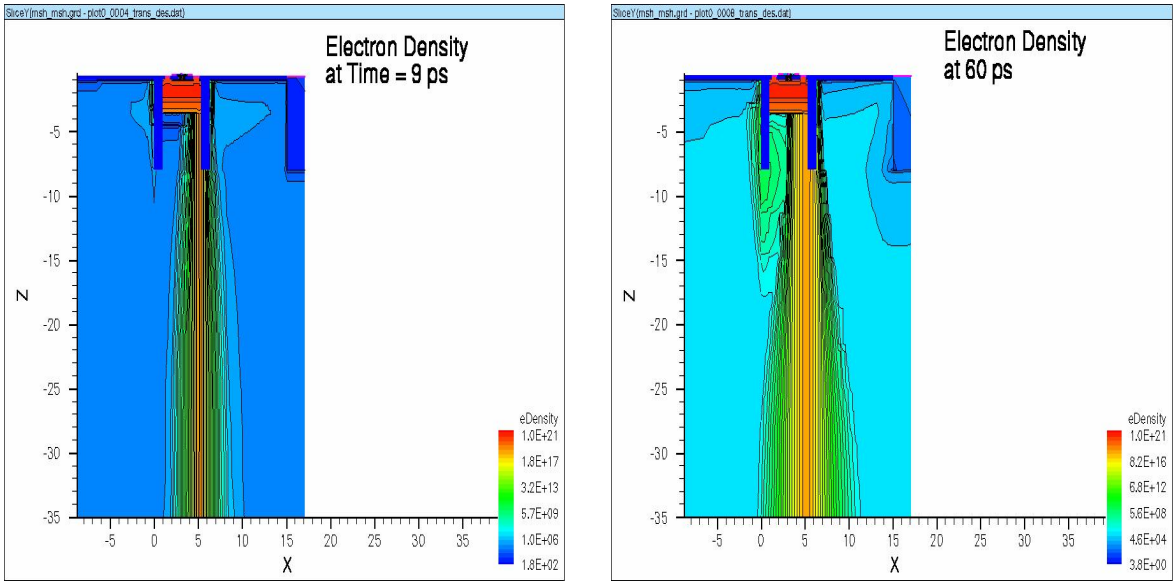
Figure 4.6: Cross section of the device showing the electrostatic potential at 800 and 4000 ps for a strike at x = 5.14 μm.

4.2.3 Contours for Angled Strike

The angled strike is necessary to be studied separately because the angled strike charge collection is different from the normal strike. Charges deposited outside the deep trench have to diffuse to the CS junction to be collected by the collector terminal.

Electrostatic Potential

In the electrostatic potential contour we can see the funneling due to the disturbance of the CS junction by the ion track.



(a) Electron Density at 9 ps (b) Electron Density at 60 ps

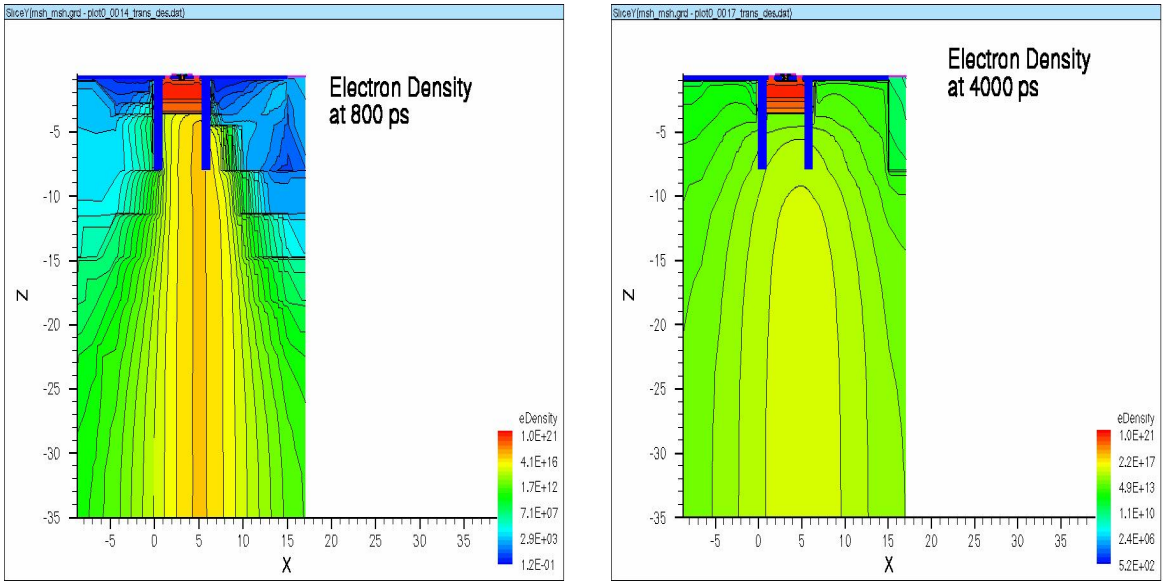
Figure 4.7: Cross section of the device showing the Electron Density at 9 and 60 ps for normal strike at x = 5.14 μm.

Fig. 4.9 and Fig. 4.10 shows the electrostatic potential at different time instants for a 30 degree ion strike at emitter center. The electrostatic potential contour at 9 ps shows the funneling of the potential as the ion track grazes the CS junction. It is not as deep as the normal strike and hence the drift collection is not as pronounced as the normal strike. At 60 ps, the funnel has widened due to the outward diffusion of the heavy density of charge track. At 600 ps, the funnel has reduced in intensity but still charges are collected by drift. At 8000 ps, the CS junction has come back to its original state. Once the funnel has come back to its original state, charges get collected through diffusion.

Electron Density

Unlike the normal strike, the electron density track passes through the intrinsic and extrinsic portions of the device in angled strike. Hence it is necessary to see the evolution of electron track with time for an angled strike.

Fig. 4.11 and Fig. 4.12 shows the electron density at different time instant for a 30 degree ion strike at the emitter center. As the time goes from 9 ps to 60 ps the ion track starts expanding



(a) Electron density at 800 ps (b) Electron density at 4000 ps μm

Figure 4.8: Cross section of the device showing the electron density at 800 and 4000 ps for a normal strike at NS Edge (x = 5.14 μm.

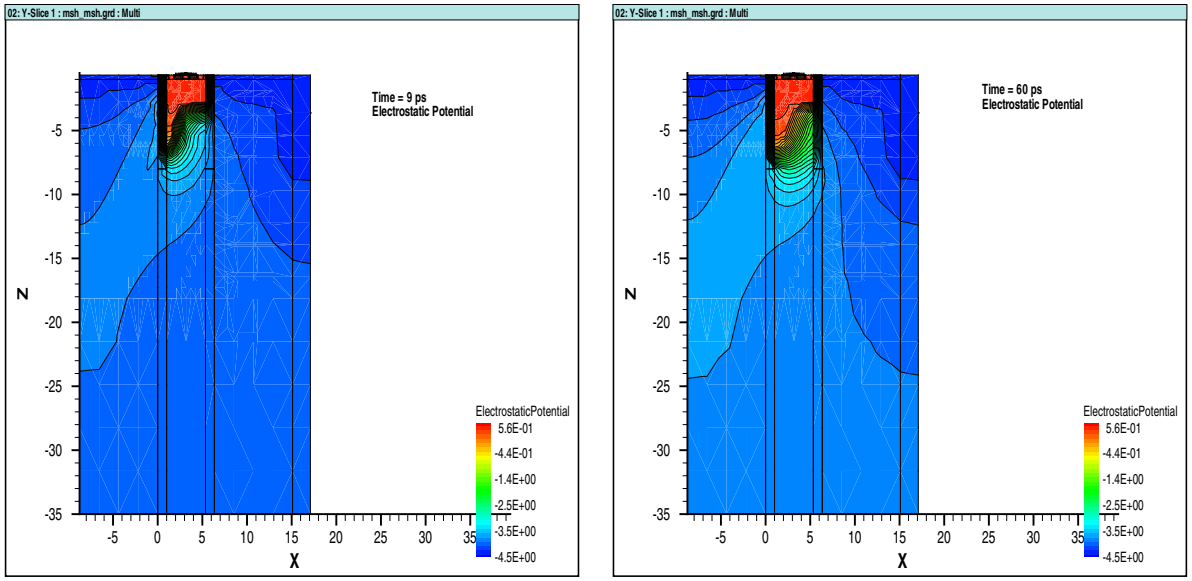
outward and hence we can see the increasing width in potential funnel. At 600 ps the ion track has expanded to the entire CS junction area. At 8000 ps, the charges has diffused to the entire device and gets collected through diffusion.

4.3 Substrate Effect

Substrate doping influences the charge collection for strikes outside DT by modifying the lifetime of the diffusing charges [28]. Fig. 4.13 shows charge collection comparison for substrate with doping 1×10^{15} cm^{-3} and 1×10^{14} cm^{-3} for regular HBT. Charge collection for N_{sub} 1×10^{14} cm^{-3} is higher than for N_{sub} 1×10^{15} cm^{-3} mainly because of the slightly increased lifetime from 9 μs to 10 μs.

4.4 Simultaneous Charge collection issues

Previous simulations were done for a stand-alone single HBT with a large simulation area of 35 × 35 μm^2. This large area is necessary due to the large lifetime and large diffusion lengths



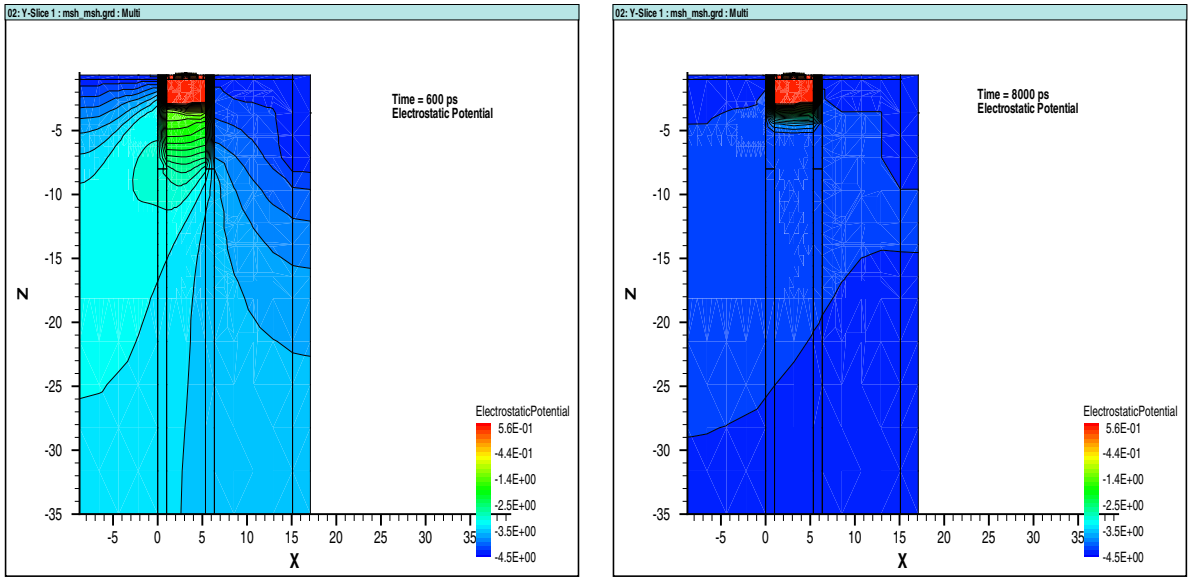
(a) Electrostatic potential at 9 ps (b) Electrostatic potential at 60 ps

Figure 4.9: Cross section of the device showing the electrostatic potential at 9 and 60 ps for 30 degree strike at emitter center.

involved. In circuits, however, the spacing between transistors is several microns, which is comparable or even less than the diffusion lengths. A single ion strike can cause charge collection in multiple devices near the strike location [29]. Thus we need to examine charge collection using realistic layout using multiple devices. Ion strike simulations are performed for normal strikes and angled strikes and the simultaneous charge collection in multiple devices are studied. Since the simulations are time consuming only limited points are simulated. Simulation parameters are the same as the stand-alone simulations. Simulation results on 2x2 and 3x3 arrays are presented below.

4.4.1 2×2 HBT Array

Fig. 4.14 illustrates the layout of a 2x2 array for regular HBTs simulated. C1, C2, C3 and C4 are the collectors of individual devices. A 5 μm spacing, typical of circuit layouts using SiGe HBT technology, is used. Normal ion strike simulations are performed at points A and B. Point A is at equal distance from all devices, and represents the outside DT strike location for maximum charge collection sharing. Point B is the center of C4, and represents inside DT strikes.



(a) Electrostatic potential at 600 ps (b) Electrostatic potential at 8000 ps

Figure 4.10: Cross section of the device showing the electrostatic potential at 600 and 8000 ps for 30 degree strike at emitter center.

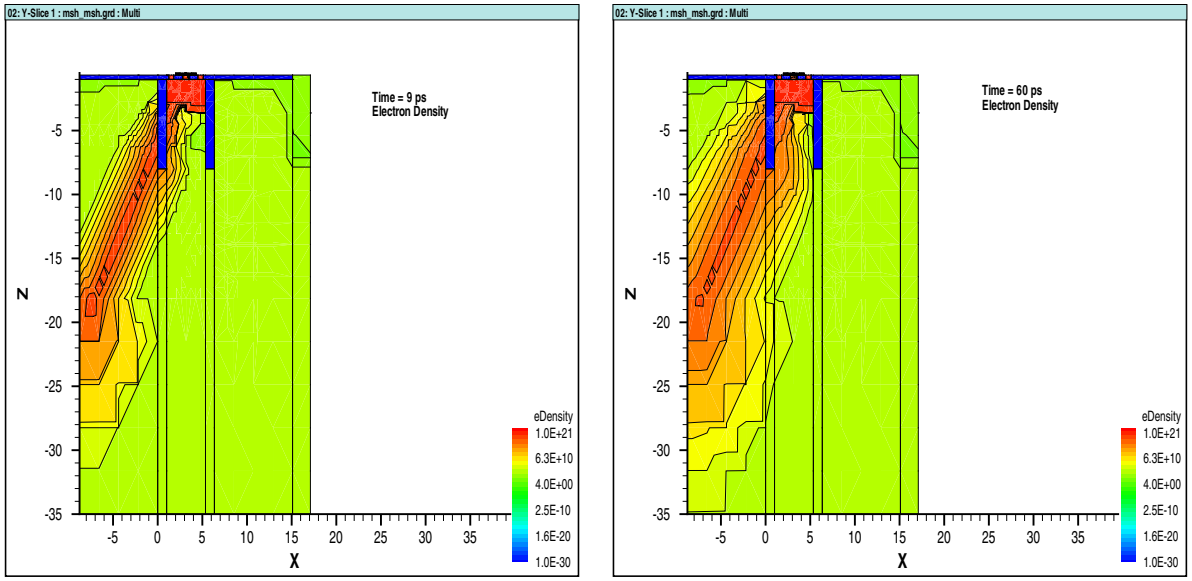
Fig. 4.15 shows the charge collection for a 2×2 HBT array for a normal ion strike at point A and point B. As expected, for a strike at point A, all the devices collect charge through diffusion. Point A is at equidistant from all the devices. Hence all the devices collect approximately the same amount of charge. For the strike at point B (at the center of device A22), the struck device C4 collects charge through drift and diffusion. A11, A12, A21 collects approximately equal amount of charge through diffusion.

4.4.2 3×3 HBT Array

Normal Strike

The normal strike is simulated at four representative points in a 3×3 array of transistors. Fig. 4.16 shows the layout of a 3×3 HBT array. A11 to A33 are the individual devices. A 5 μm spacing, typical of circuit layouts using SiGe HBT technology, is used. Normal ion strike simulations are performed at point 1, 2, 3 and 4 and charge collection examined.

Fig. 4.17 gives the charge collection by all the devices for normal strike at Point 1 and Point 2. Point 1 is located inside the DT of A32. For a strike at point 1, A32 collects charge through drift



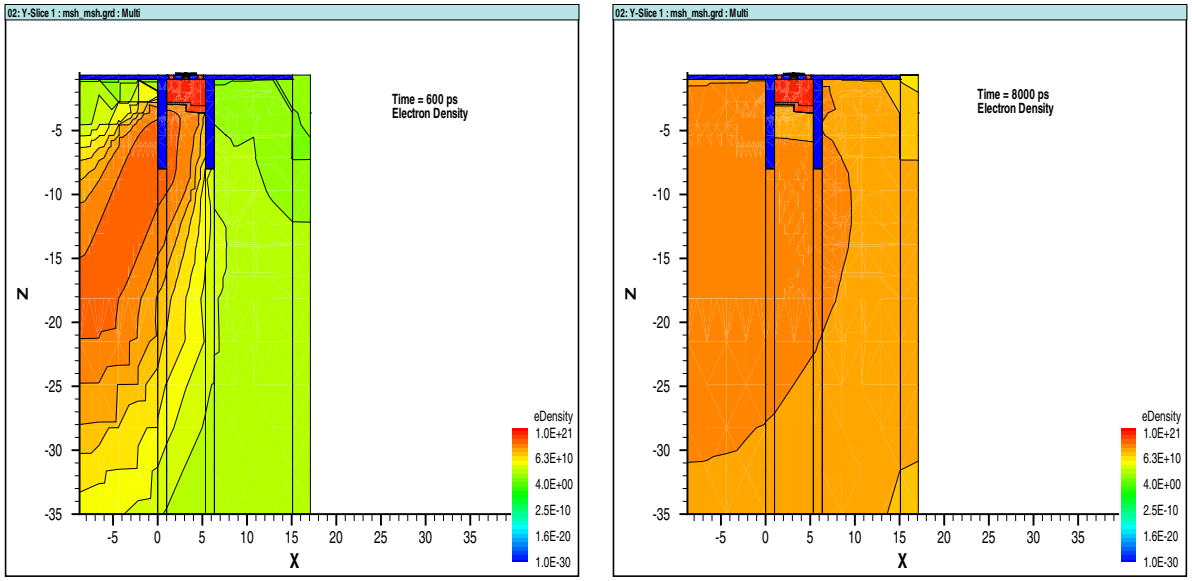
(a) Electron Density at 9 ps (b) Electron Density at 60 ps

Figure 4.11: Cross section of the device showing the Electron Density at 9 and 60 ps for 30 degree strike at emitter center.

initially. Once the drift collection by A32 is complete, diffusing charges are collected by the struck and the neighbouring devices. All the neighbouring devices collects an average charge of 0.3 pC, which is high enough to cause an upset. Point 2 is located in the silicon region between A32 and A22. The strike at point 2 leads to collection of charge through diffusion by the neighbouring devices. From the figure we can see that the transistors A32 and A22 starts collecting at 2 ns due to the proximity to the strike. All other devices start collecting only by 80 ns.

Fig. 4.18 shows the charge collection for normal ion strike at Point 3 and Point 4. The charge collection characteristic for Point 3 is similar to Point 1 and Point 4 is similar to Point 2. The difference is the devices near the ion track.

Fig. 4.19 and Fig. 4.20 shows the electron density contour for a normal strike at point 2. At 0.1 ns we can see the ion strike location and the diffusion of charges to the transistors in the neighbouring devices. At 0.7 ns the diffusion has reached to the devices in the other end of the array but it has not yet diffused into the entire array. We can still see the heavy charge at the ion strike location at 1 ns and the charges have diffused further. At 3 ns the charges has diffused into the



(a) Electron density at 600 ps (b) Electron density at 8000 ps

Figure 4.12: Cross section of the device showing the electron density at 600 and 8000 ps for a 30 degree strike at emitter center.

entire array. From these figures we can see that the diffusion of charges initiate charge collection in the neighbouring devices first and then the farther devices start collecting charge.

4.4.3 Angled Strike

Ion strike simulations were performed on the 3 × 3 HBT array at incident angles $\theta = 30\,^{\circ}$ and $45\,^{\circ}$. Fig. 4.21 shows the position of angled ion incidence. At each position, simulations are performed for both angles $\theta = 30\,^{\circ}$ and $45\,^{\circ}$.

Fig. 4.22 shows the terminal charge collection for an ion strike at point 1 at angles $30\,^{\circ}$ and $45\,^{\circ}$. The ion path strike passes through the CS junction of A32 for $30\,^{\circ}$ and grazes the junction for $45\,^{\circ}$. So we can see a heavy drift for $30\,^{\circ}$ than the $45\,^{\circ}$. A31 is in the path of the ion track. As the angle of incidence increases, the ion track comes nearer to the CS junction of A31 as shown in fig. 4.23. Hence we can see higher charge collection in A31 for $45\,^{\circ}$. All other devices collect charge through diffusion.

Fig. 4.24 gives charge collection for an ion strike at point 2 at angles $30\,^{\circ}$ and $45\,^{\circ}$. The strike point is located between the devices A32 and A22. The charge collection by all transistors

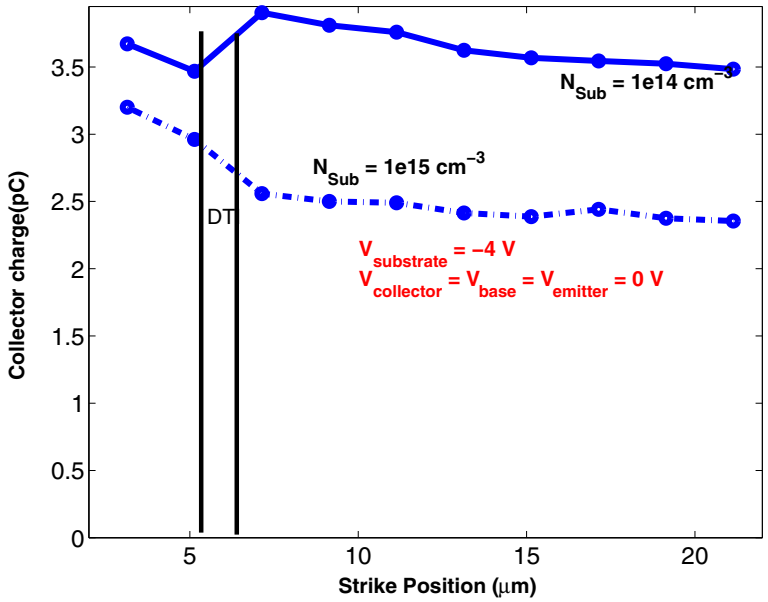


Figure 4.13: Collector charge comparison between substrate doping of 1×10^{15} cm^{-3} and 1×10^{14} cm^{-3}. Comparison is done for a normal strike.

is through diffusion. Transistors A32, A22, A31 and A21 are the immediate neighbours to the ion track. So these devices starts collecting charges at 5 ns. All other transistors start collecting charge by 100 ns.

Point 3 has a similar characteristics to Point 1. The role of A31 and A32 are played by A21 and A22 respectively.

Fig. 4.25 gives the charge collection for the ion strike at point 4 at angles 30 ° and 45 °. Point 4 is inside the DT of A23. The struck device collects charge through heavy drift for a strike at incidence 30 ° than 45 °. As the strike angle increases, we can see an enhanced charge collection by the devices on the path of the ion track. This is because the ion track comes closer to the CS junction of the neighbouring devices as shown above.

Fig. 4.26 gives the charge collection for ion strike at point 5. Point 5 is located in between A23 and A13. The ion track is located in between A22, A23 and A12, A13. Hence these devices start collecting charge first. Then all other devices start collecting once the charge has diffused to the entire structure.

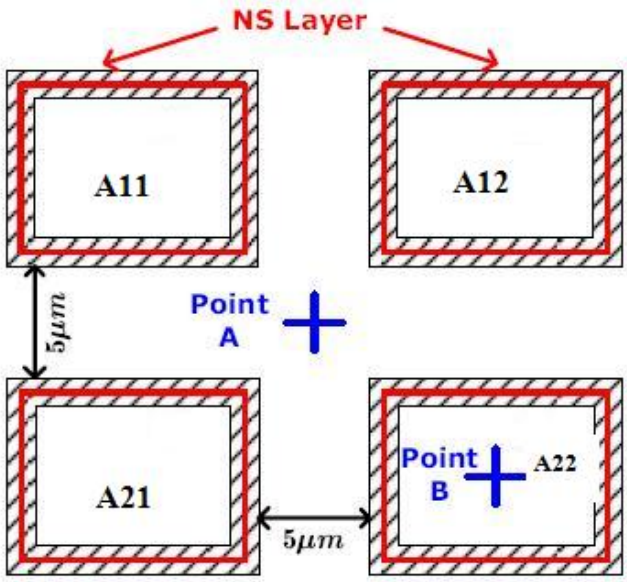


Figure 4.14: Layout of a 2×2 HBT array showing the representative points for a normal strike. NS layers for each transistor is marked by a red line.

Fig. 4.27 and Fig. 4.28 shows the electron density contour for an ion strike inside A32 at 30 °. At 0.1 ns, the electron density has diffused to the neighbouring devices A31, A21 and A22. Further diffusion takes place at 1 ns to the devices A11, A12, A33 and A23. The charges are diffused to all the devices at 3 ns and at 10 ns the entire substrate is filled with the excess electron density.

Hence we can see that the mode of charge collection (drift or diffusion) depends on the position of ion strike and the charge collection time depends on the distance of the device from the ion strike location and the angle of ion strikes. From the above discussions diffusion is the main mode of charge collection in multiple devices, especially for angled strikes. Hence the hardening design should aim at reducing the diffusive charge collection. The next chapter discusses radiation hardening by design, where a dummy CS junction is introduced, which decreases charge collection by diffusion.

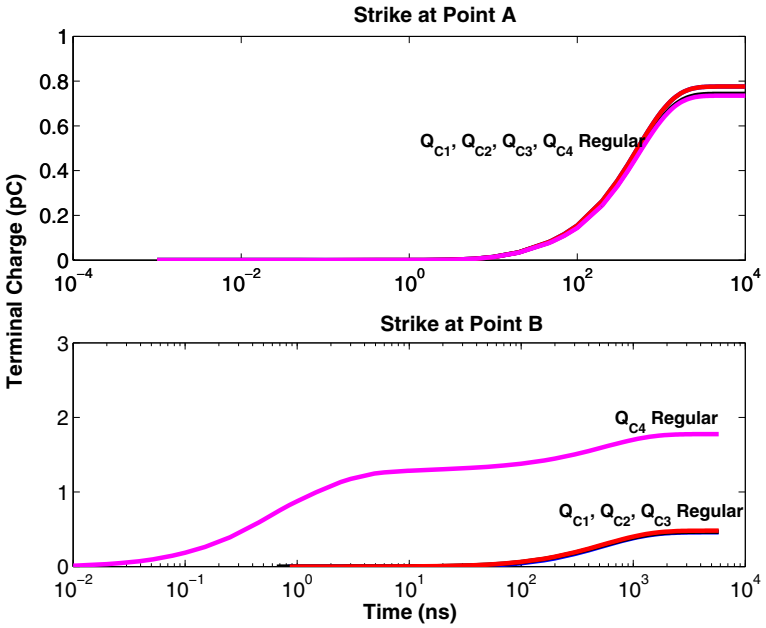


Figure 4.15: Charge collection for a strike at Point A and Point B for a regular 2×2 HBT array.

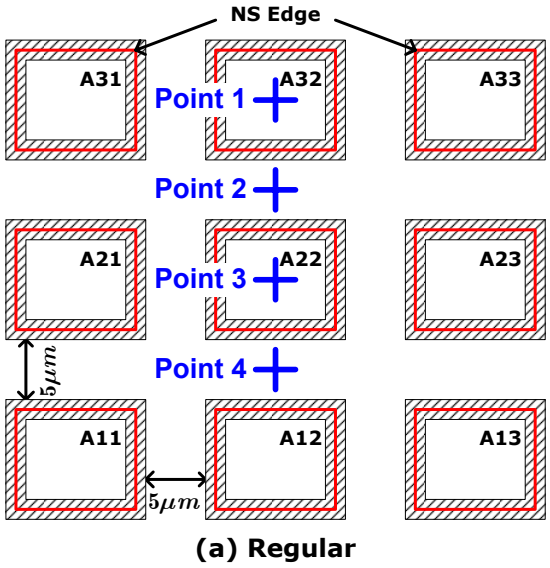
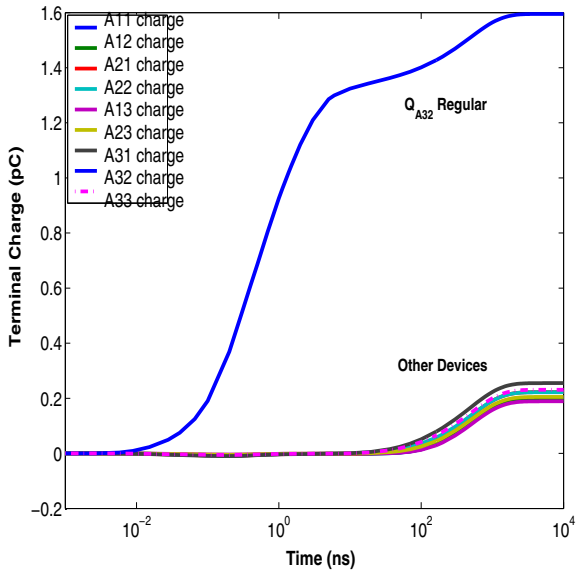
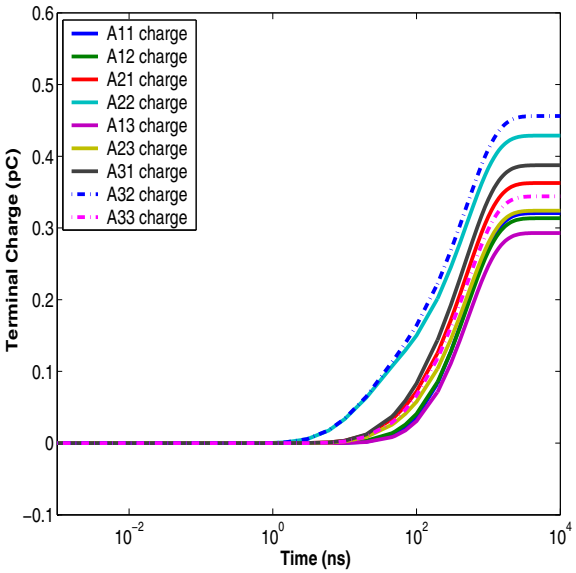


Figure 4.16: Layout of a 3×3 HBT array showing the representative points for a normal strike. NS layers for each transistor is marked by a red line.

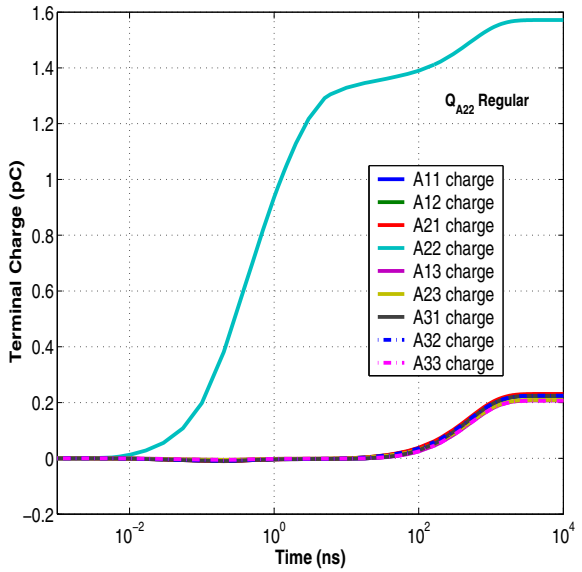


(a) Ion strike at point 1

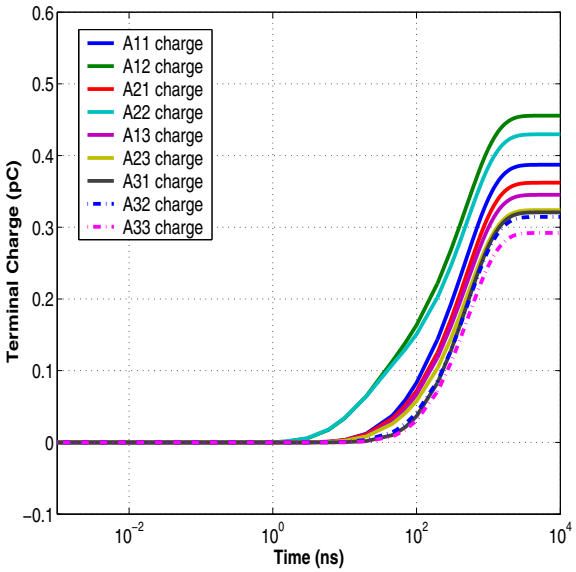


(b) Ion strike at point 2

Figure 4.17: Terminal charge for normal ion strikes at point 1 and point 2.

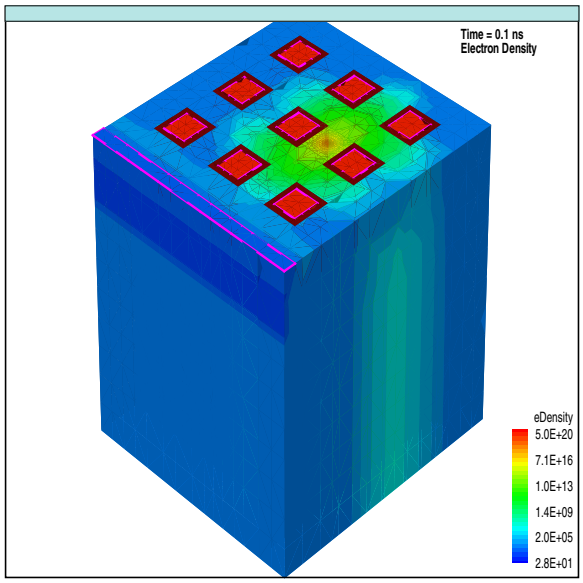


(a) Ion strike at point 3

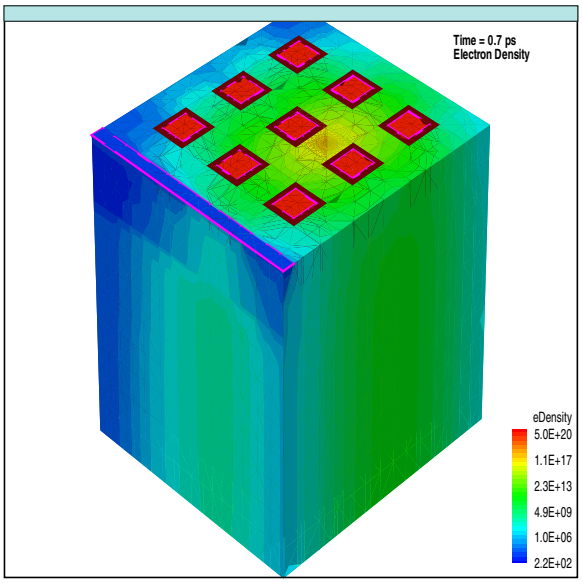


(b) Ion strike at point 4

Figure 4.18: Terminal charge for normal ion strikes at point 3 and point 4.

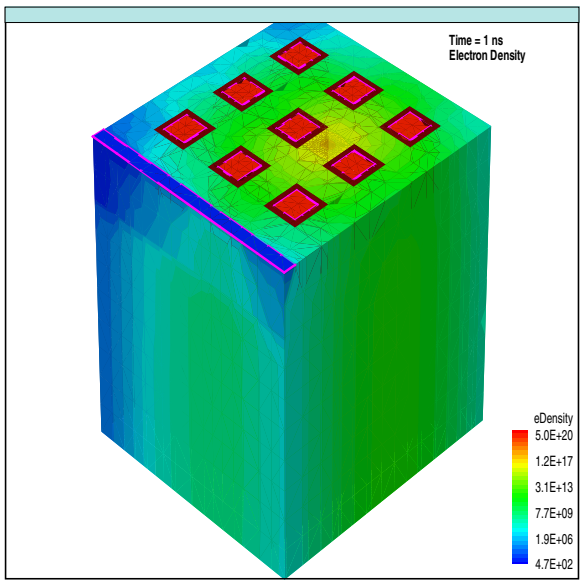


(a) Electron density contour at 0.1 ns

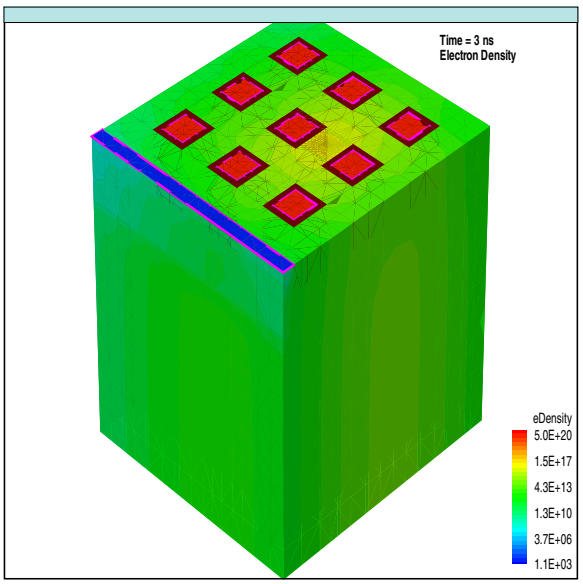


(b) Electron density contour at 0.7 ns

Figure 4.19: Electron density contour for a normal strike at point2 (between A32 and A22) at 0.1 ns and 0.7 ns.

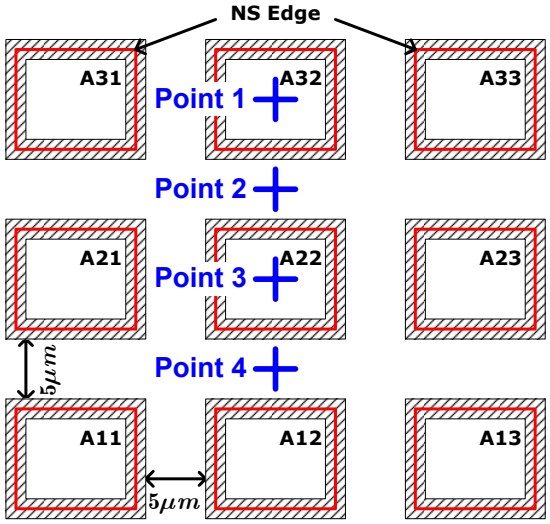


(a) Electron density contour at 1 ns



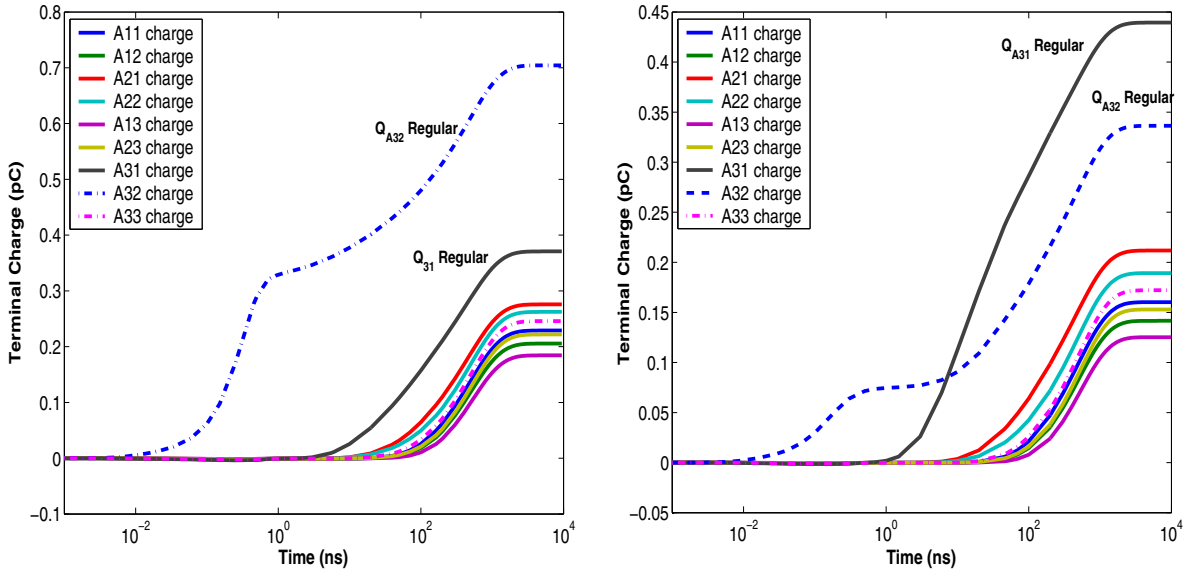
(b) Electron density contour at 3 ns

Figure 4.20: Electron density contour for a normal strike at point2 (Between A22 and A32) at time 1 ns and 3 ns.



(a) Regular

Figure 4.21: Layout of a 3×3 HBT array showing the representative points for an angled strike. NS layers for each transistor is marked by a red line.



(a) 30 ° (b) 45 °

Figure 4.22: Terminal charge for an ion strike at point 1.

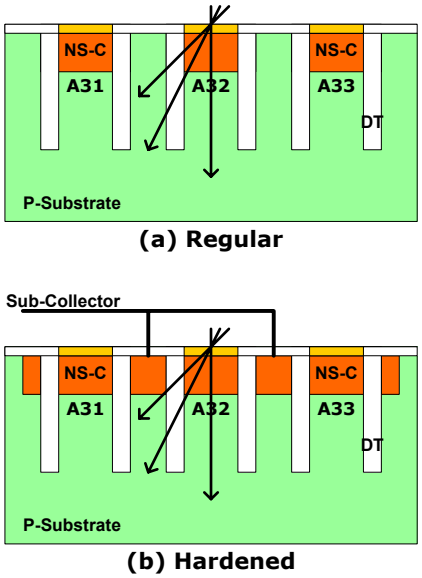


Figure 4.23: A cartoon illustration of the cross section of the regular HBT array showing the devices A31, A32 and A33 (not to scale). The ion path represents the normal and angled strikes.

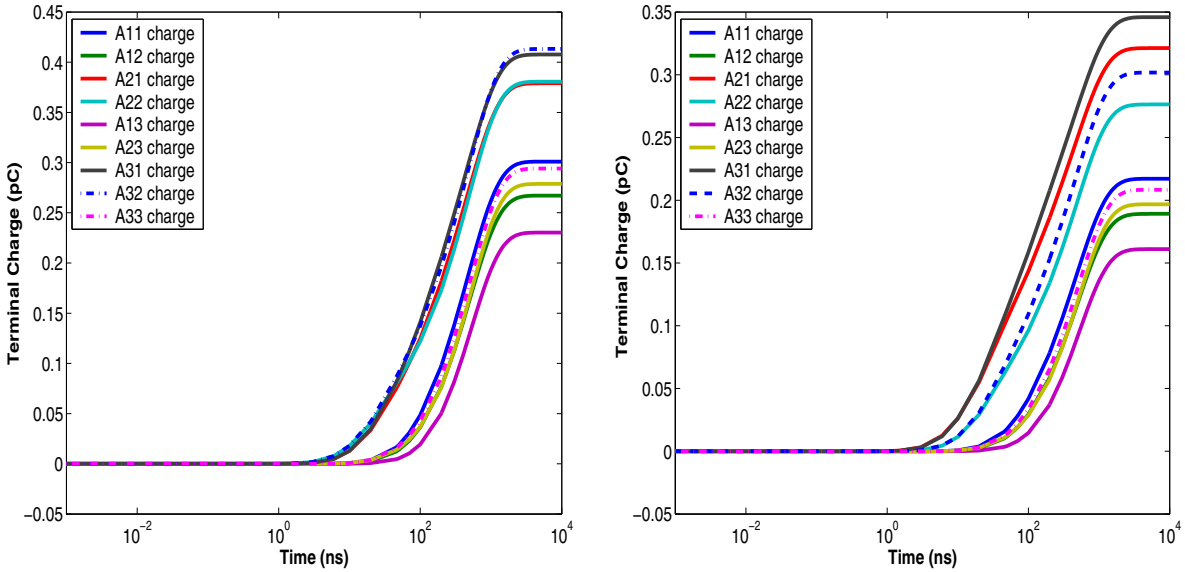
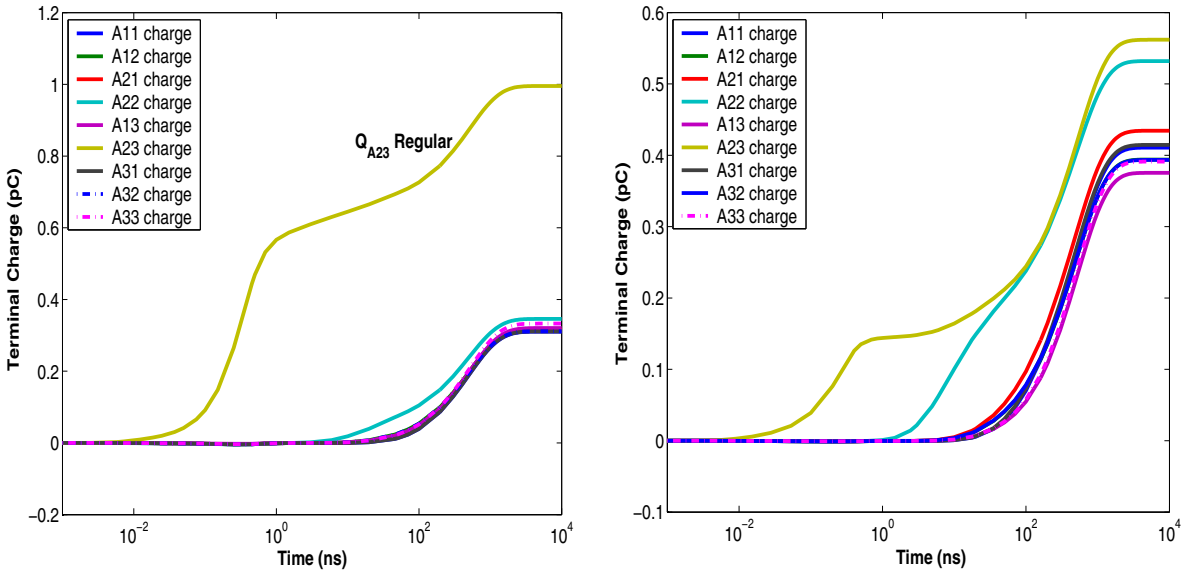
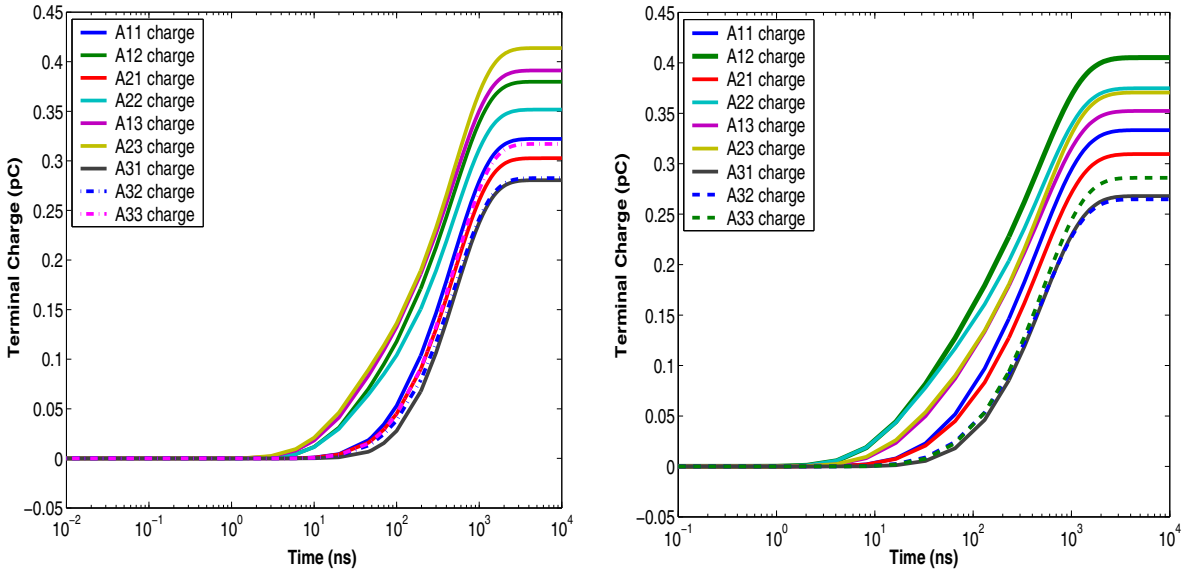


Figure 4.24: Terminal charge for an ion strike at point 2.



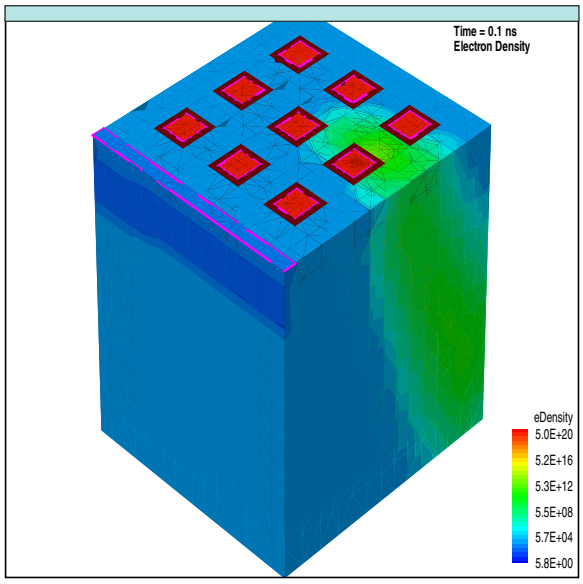
(a) 30 ° (b) 45 °

Figure 4.25: Terminal charge for an ion strike in the device A23.

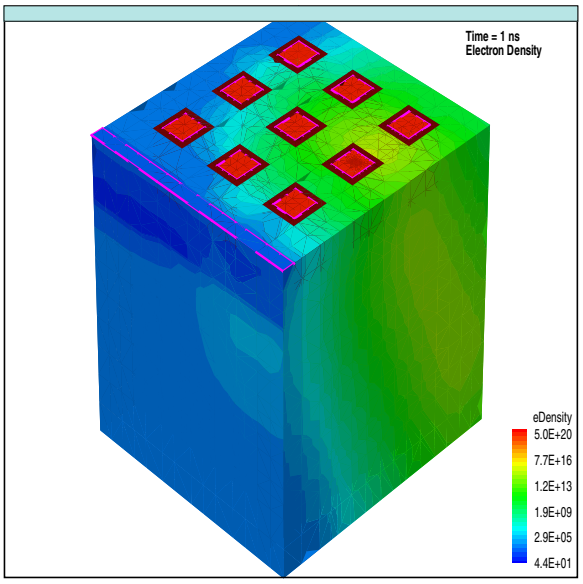


(a) 30 ° (b) 45 °

Figure 4.26: Terminal charge for an ion strike in the silicon region between A23 and A13.

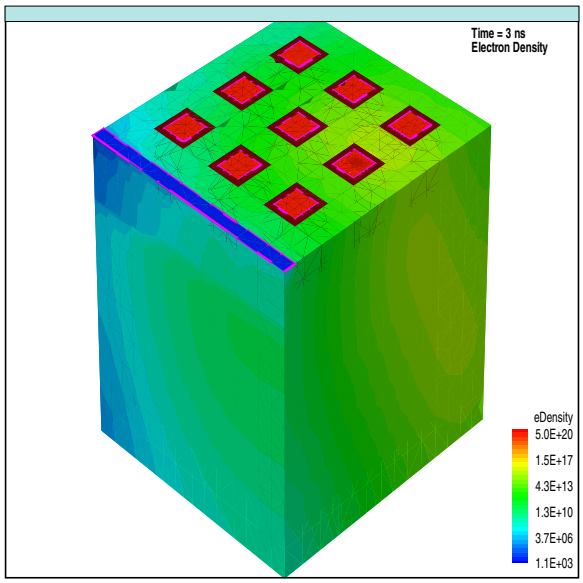


(a)Electron density contour at 0.1 ns

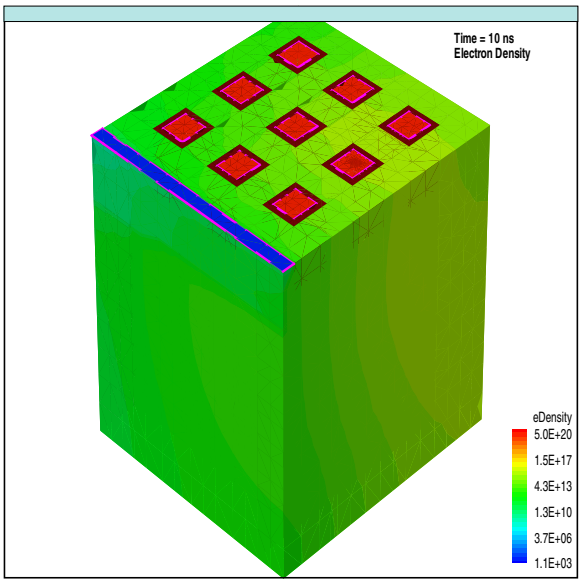


(b)Electron density contour at 1 ns

Figure 4.27: Electron density contour for an ion strike at Point 1, which is located inside N8.



(a)Electron density contour at 3 ns



(b)Electron density contour at 10 ns

Figure 4.28: Electron density contour for an ion strike at Point 1, which is located inside N8.

Chapter 5

Radiation Hardening By Design

In Radiation Hardening By Design (RHBD), electronic components are manufactured to meet specified radiation performance criteria, but the techniques employed to meet these criteria are implemented either in layout or in the application architecture and not in the fabrication process. RHBD is typically considered distinct from radiation-hardening-by-process (RHBP). Radiation hardening via process modifications is the traditional approach used by rad-hard foundries. While RHBP has the advantage of being an extremely reliable means of achieving hardened components, RHBP is susceptible to low volume concerns such as yield, process instability, and high manufacturing costs. These drawbacks, when coupled with the post Cold War contraction of the government electronics market, caused a dramatic industrial exodus from rad-hard manufacturing. In order to leverage the economy-of-scale provided by the commercial electronics industry, some rad-hard electronics customers are looking at RHBD as a potentially lower cost solution to persistent radiation threats. The RHBD approach makes sense in todayÐs evolving electronics marketplace where semiconductor fabrication is becoming more detached from integrated circuit design. Various hardening techniques like introduction of a back junction [30] or a heavily doped p-layer [31] or SOI technology [23] have been proposed to reduce charge collection. But all these techniques require process changes. The structures proposed in this chapter requires only layout changes. In this chapter a new SEU hardening approach that reduces charge collection by the use of a dummy collector-substrate junction is proposed [32]. This chapter deals with different layouts and comparison of charge collection between the various layouts.

5.1 Device Structure and Layout

The cross section and layout of a regular 8HP HBT were already shown in Chapter 2 (see Fig. 2.1 and Fig. 3.1). The deep trench encloses the active device and the NS layer defines the N^+ subcollector. The silicon area inside DT determines the CS junction area. During SEU, the CS junction either directly collects the deposited charges through drift within the potential funnel or indirectly collects charges after they arrive at the junction after diffusion. The diffusion length of the carriers is in the order of tens of microns or more. Hence a dummy CS junction should be able to reduce the amount of diffusive charge collection by the HBT collector. The dummy CS junction can be placed inside DT or outside DT. If the dummy CS junction is placed inside DT, then some distance should be maintained between the CS junction and the dummy CS junction. This distance leads to area penalty in the device structure. As we will see in this chapter, placing the dummy CS junction inside DT does not provide any radiation hardening. The next option is placing the dummy CS junction outside the DT, surrounding the perimeter of the DT.

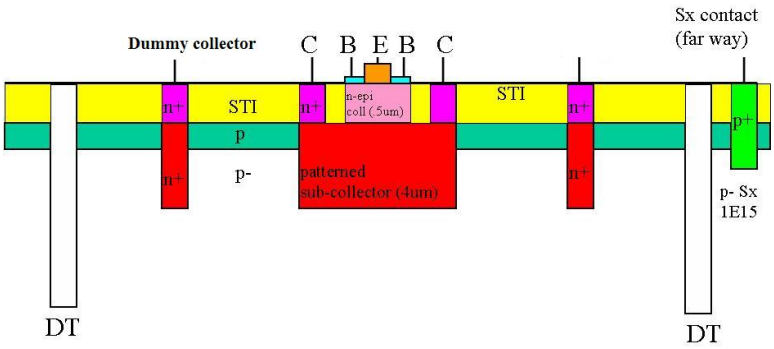


Figure 5.1: Dummy cross section of the device with the dummy CS junction placed inside the DT. Drawn not to scale.

Fig. 5.1 shows the cross section of the device with the dummy collector inside the DT. We can see a lot of area penalty inside the DT area. As will be seen, this device does not give a radiation hardened device.

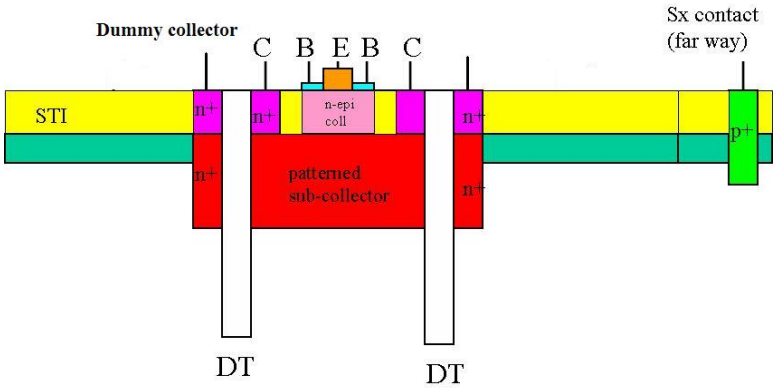


Figure 5.2: Dummy cross section of the device with the dummy CS junction placed outside the DT. Dummy collector surrounds the deep trench isolation. Drawn not to scale.

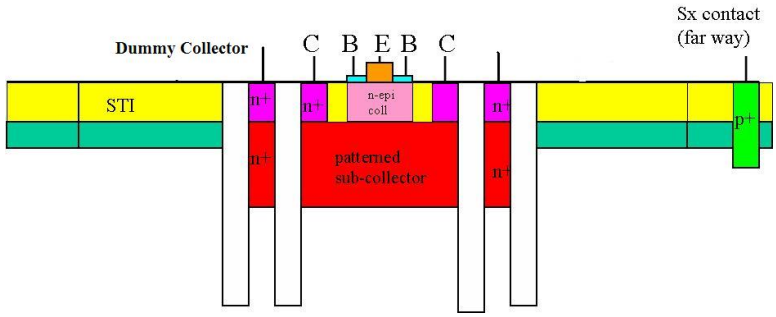


Figure 5.3: Dummy cross section of the device with the dummy CS junction placed outside the DT. The dummy CS junction is surrounded by a second DT, surrounding the dummy collector. Drawn not to scale.

Fig. 5.2 and Fig. 5.3 shows the cross section of devices with the dummy collector outside the DT. The difference between both figures is that in the Fig. 5.2 the dummy collector surrounds the DT enclosing the intrinsic portion of the device but in Fig. 5.3 the dummy collector is surrounded by a second deep trench. In these structures the dummy junction can be obtained by pulling out the NS layer in the regular HBT so that the NS encloses the outer DT edge by an amount W_d. The dummy NS outside the DT is contacted through the same N^+ sinker used for contacting the transistor NS. Fabrication of the hardened HBT is done with a few layout changes. For a stand-alone device one may be concerned about the extra silicon area. In integrated circuits, however,

the proposed hardening approach does not really suffer area penalty. Devices are apart by several microns due to design rules, density requirement and other practical reasons. The unused silicon between the neighbouring devices can be utilized to create the dummy collector.

5.2 Simulation Strategy and Parameters

We first consider stand-alone single device, like those used in device characterization and microbeam testing. Devices are separated by 100 μm or more. The transistor active area is very small compared to the area needed for pads and interconnection leading to the transistor terminals. Due to thick overlayer, current heavy ions available for microbeam testing cannot provide deep strike, particularly for angled incidence. Therefore, at present, 3-D simulation is the only viable way of examining charge collection for deep strikes and large angled strikes. Charge track generation and physical models are the same as used in chapter 2. Deep strikes with an LET of 0.1 pC/μm are simulated. A LET of 0.1 pc/μm is equivalent to 9.7 MeV-cm^2/mg. The default SRH recombination model parameters are used here, unlike chapter 2 where the SRH recombination parameters are changed to fit the microbeam data. The default parameters give a longer lifetime to the carriers. With the default parameters, the carriers have a lifetime of 9 μs for a substrate doping of 1×10^{15} cm^{-3}. It represents the worst case because charges deposited outside DT gets collected because of the longer lifetime. Collector, emitter and base terminals are grounded and the substrate is biased at -4 V. The dummy terminal bias is varied from 0 to 4 V and as will be seen there was no bias effect on charge collection. Hence for all simulations a dummy collector bias of 3 V was used.

5.3 Device With Shared Dummy Collector Inside DT

The dummy collector-substrate junction is fabricated inside DT. This design gives area penalty inside the active device area. Is this area penalty a good compromise to the radiation hardening? The regular HBT and the dummy collector HBTs are aligned at the DT edge and hence the ion strike location is similar in both HBTs. The charge collection is compared at four representative points:

- Emitter center.
- NS Edge.
- Dummy collector center.
- Outside DT.

The LET used in these simulations are 0.0478 pC/μm and the strike is deep strike. The charge collection is compared between the regular HBT and hardened HBT.

5.3.1 Emitter center strike

The charge collection is compared between the regular HBT and the hardened HBT for an ion strike at the emitter center. Fig. 5.4 shows the collector charge comparison between regular HBT

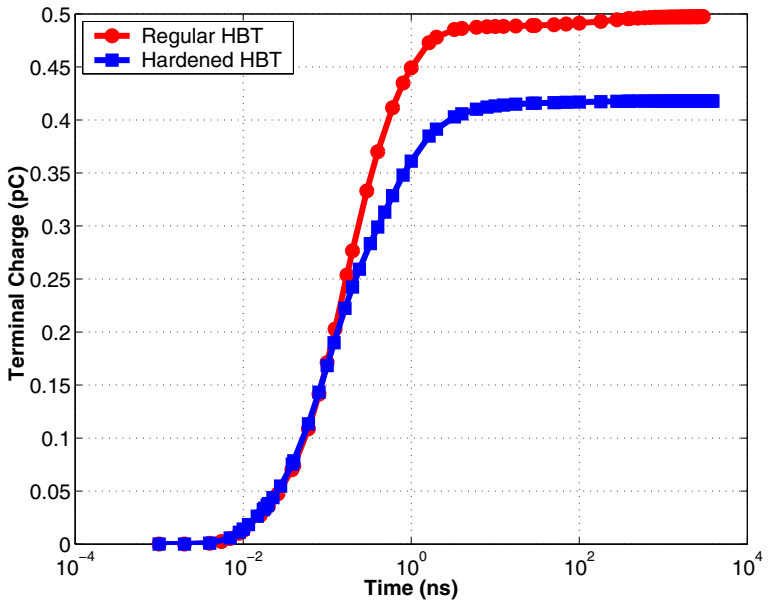


Figure 5.4: Collector charge comparison between Regular and dummy collector inside DT HBT. This figure is for an ion strike at the emitter center.

and the hardened HBT. The hardened HBT collects 0.08 pC less than the regular HBT. This is not a really good improvement in charge collection reduction.

5.3.2 NS Edge Strike

The NS edge is located at the interface between the subcollector and DT. Collector charge collection is compared between the regular HBT and hardened HBT. Fig. 5.5 shows the collector

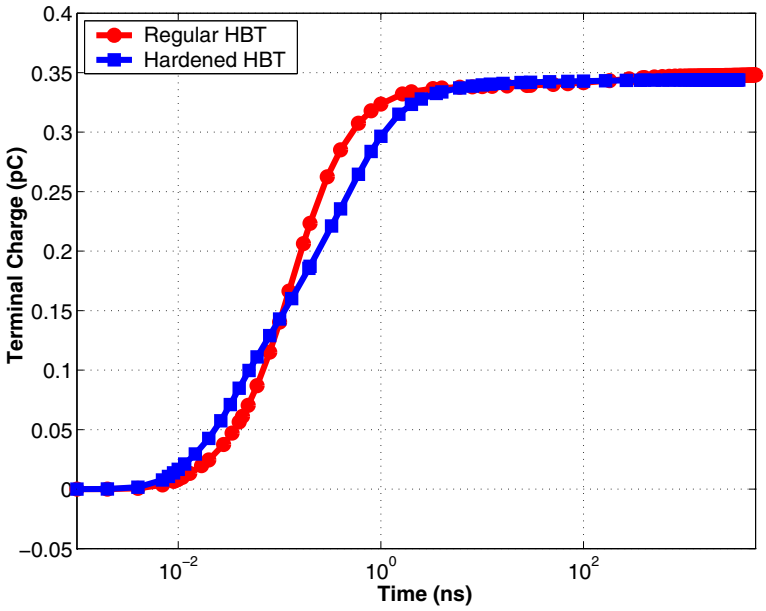


Figure 5.5: Collector charge comparison between Regular and Shared dummy collector inside DT HBT. This figure is for an ion strike at the NS Edge.

charge comparison for an ion strike at the NS edge. We can see that there is no difference in charge collection between the regular and hardened HBT.

5.3.3 Shared dummy collector center strike

The ion strike position is located in the center of the dummy collector. In the regular HBT, the ion strike position is at the same position as in the hardened HBT. Fig. 5.6 shows the collector charge comparison for an ion strike at the dummy collector center. The charge collection in the hardened HBT is more due to the funneling in the dummy CS junction. We can clearly conclude that the hardened HBT has no radiation hardening.

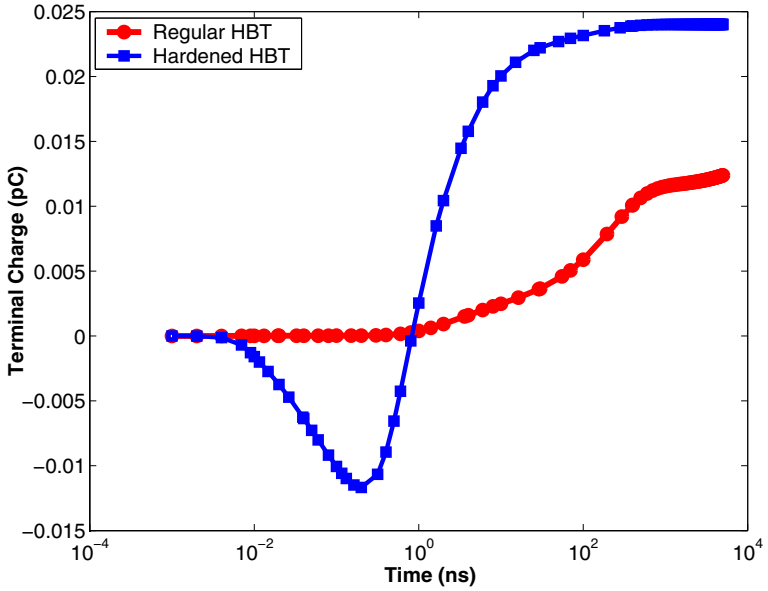


Figure 5.6: Collector charge comparison between Regular and dummy collector inside DT HBT. This is for an ion strike at the dummy collector center.

5.3.4 Outside DT strike

The ion strike position is located outside the DT. In the regular HBT, the ion strike position is at the same position as in the hardened HBT. Fig. 5.7 shows the collector charge comparison for an ion strike outside DT. The charge collection difference between the regular and hardened HBT is very less, which implies that the hardened HBT does not provide a good hardening. Thus we can conclude that the presence of the dummy collector inside the DT does not give any radiation hardening, in spite of the area penalty.

Fig. 5.8 gives the charge collected by the dummy collector of the device. The charge collected for the strike at the dummy collector center is more due to the presence of drift collection. This drift collection is due to the funneling of the dummy CS junction. For all other strikes the charge collected is approximately the same.

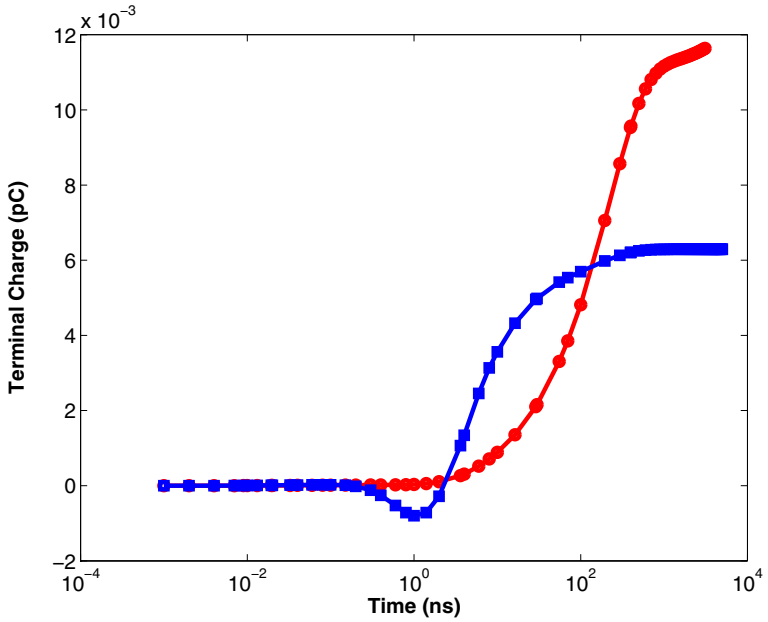


Figure 5.7: Collector charge comparison between Regular and dummy collector inside DT HBT. This is for an ion strike outside DT.

5.4 Shared Dummy Collector located outside DT

In the layout, the dummy collector is placed outside the DT, along the perimeter of the DT. Two structures were proposed: In one structure the dummy collector was placed outside DT and in the other one the dummy collector is placed outside DT and is surrounded by another DT as shown in the cross section. The collector charge collection is compared between the regular HBT and the hardened HBTs. The collector charge is compared because it is the sensitive node in most of the circuits. Simulations are performed for strikes along the x-axis with y fixed at the center of the device. At each incident position, simulations are done for incident angles of $\theta = 0°$, 30°, 45°, and 60°.

5.5 Normal Strike Comparison

The devices are aligned at the DT edge and hence the ion strike locations represent the same point in the three device. Fig. 5.9 shows the ion strike locations in a 2-D cross section of the single

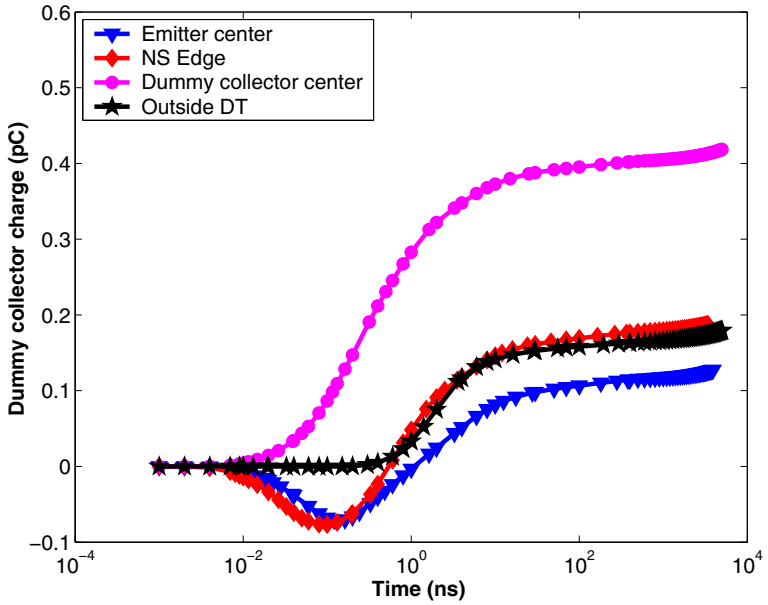


Figure 5.8: Dummy collector charge comparison between Regular and dummy collector inside DT HBT. This is for an ion strike outside DT.

DT hardened HBT.

Fig. 5.10 gives the normal strike charge collection comparison between the regular and single DT hardened HBT (SDT) and double DT hardened HBT (DDT). Simulations were performed for different dummy collector widths (W_d). The collector charge is approximately the same for W_d = 1, 2 and 3 μm. The spacing between adjacent devices in circuits using SiGe HBTs must be a minimum of 5 μm. Hence it is more than sufficient to place the dummy collector, without any area penalty. We note that the actual dummy CS junction area is larger than what W_d indicates. This is because of the existence of lateral junction between the N^+ sub-collector and the surrounding p-substrate.

The Double DT hardened HBT collects less charge compared to the regular HBT for strikes inside and outside DT. The single DT hardened HBT collects less charge compared to the double DT for both strikes inside and outside DT. So we can conclude that the single DT hardened HBT is more radiation hardened than the double DT for normal strike.

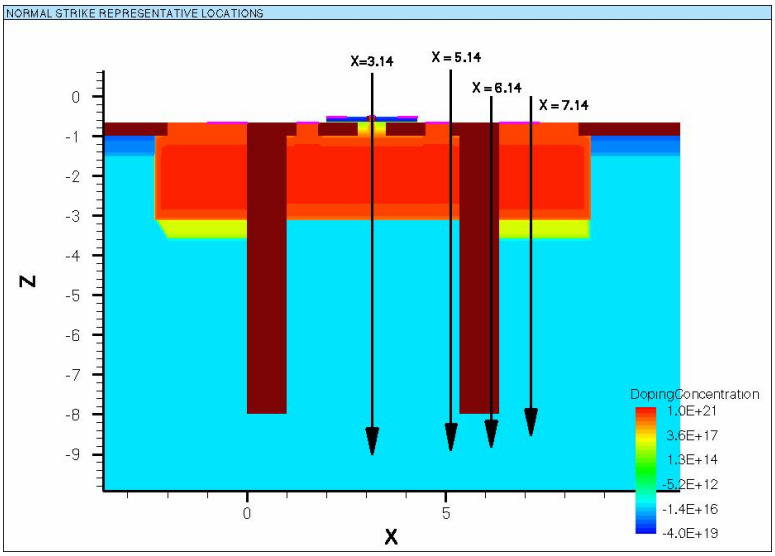


Figure 5.9: 2-D cross section of the single DT hardened HBT showing the ion strike location.

To further understand the these results, we plot charge collection versus time at representative locations as shown in Fig. 5.11. For the emitter center strike, the charge collection curve for the regular HBT shows two distinct regions: drift and diffusion as shown in Fig. 5.11(a). The final collector charge is 3.5 pC, 2.5 pC and 1.71 pC for the regular, double DT hardened and single DT hardened HBTs. The total charge collected with hardening (Q_{dummy}+$Q_C$hardened) is higher than Q_C in the regular HBT. The drift portion of the curves are approximately the same in regular and hardened HBTs. The charges left in the substrate after drift collection start to diffuse outward towards the extrinsic portion of the device. In the hardened HBTs, the diffusive charge collection is dominated by the dummy CS junction, as evidenced by the saturation of $Q_C$hardened and the increase of Q_{dummy} in Fig. 5.11(a). This leads to less charge collection by the CS junction of the active device. Fig. 5.11(b) shows charge collection versus time curves for a strike at the NS edge. The charge collection characteristic is similar to those of the emitter center strike. Again, the dummy CS junction dominates the diffusion charge collection.

For strikes outside DT, charge collection in the regular HBT is only through diffusion of charges generated outside DT towards the CS junction inside DT. Fig. 5.11(c) shows such a strike

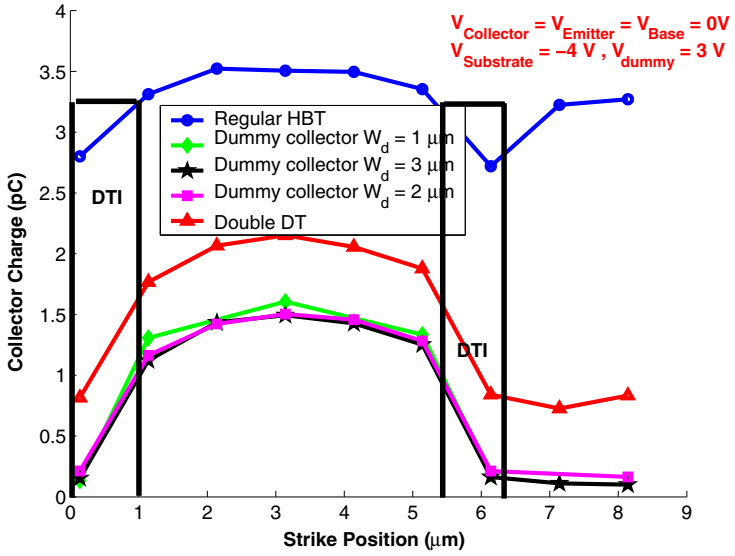


Figure 5.10: Normal strike collector charge comparison between the regular HBT, single DT hardened HBT and double DT hardened HBT.

that is on the dummy collector. As expected, the dummy collector component has a large drift component. The dummy collector collects 3.5 pC charge in single DT hardened HBT and 2.5 pC in double DT hardened HBT, and reduces the collector charge from 3.2 pC in the regular HBT to 0.17 pC in the single DT hardened HBT and 0.73 pC in double DT hardened HBT.

Fig. 5.13 and Fig. 5.14 shows the electron density contour in a single DT hardened HBT for an ion strike at the NS edge. The electron charge density diffuses outward as time evolves. Unlike the regular HBT, we can see that charge is continuously collected by the dummy CS junction. This causes more charge diffuse outward and reducing the charge available for collector terminal. For all normal strikes, with hardening, the drift component of charge collection approximately the same, while the diffusion charge collection component is nearly completely compressed.

5.6 Angled Strike Comparison

In space applications, most of the heavy ion strike occurs at large angles. So we examine the mechanisms of angled incidence charge collection. Fig. 5.15 shows the angle strike comparison

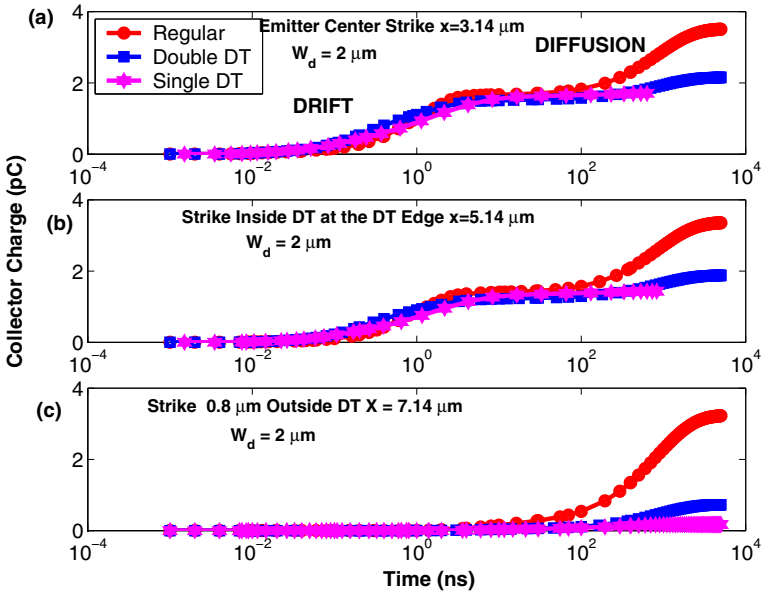


Figure 5.11: Collector charge collection characteristics for ion strike at (a) emitter center (b) DT edge and (c) Outside DT between the regular and hardened HBTs.

for $\theta = 30°$, $45°$ and $60°$. The single DT hardened HBT collects less charge than the regular and double DT hardened HBT for all strike angles and strike positions. The area of higher charge collection is reduced considerably in the hardened HBTs. The improvement from hardening is overall more significant compared to normal incidence and can be understood as follows. For normal incidence, the ion passes through either the transistor CS junction or the dummy CS junction. For large angle incidence, the ion either passes through one junction or misses both the CS junctions. Consequently, charge collection by the transistor CS junctions is mainly through diffusion in most cases and the dummy CS junction becomes more effective.

Fig. 5.16 shows the collector charge collection characteristics for ion strike at representative points. The charge collection is compared for incident angles 30° and 45°. For the strike at the emitter center, the ion track grazes through the CS junction for $\theta = 30°$, which gives a drift component. For $\theta = 45°$, although the ion track passes through the active device, it does not pass through the CS junction which leads to collection through diffusion only. Although the double DT hardened HBT has a reduced charge collection than the regular HBT, it still has a considerable amount

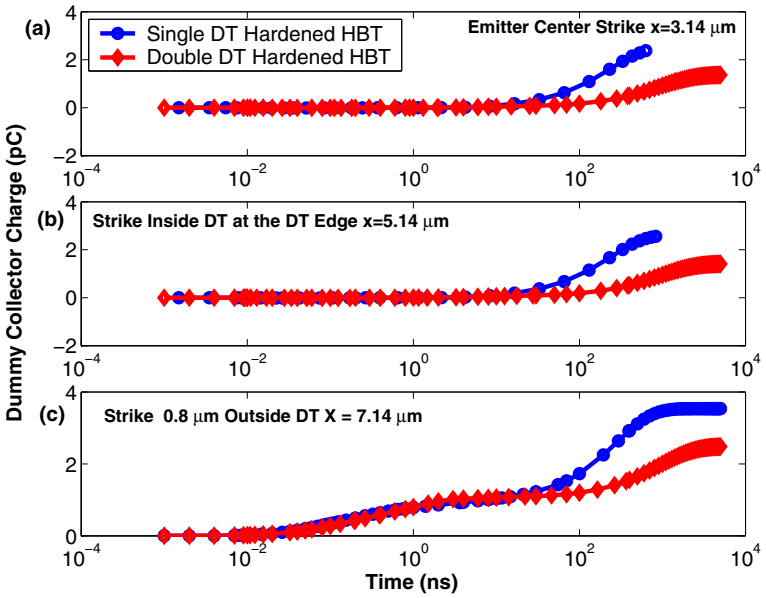
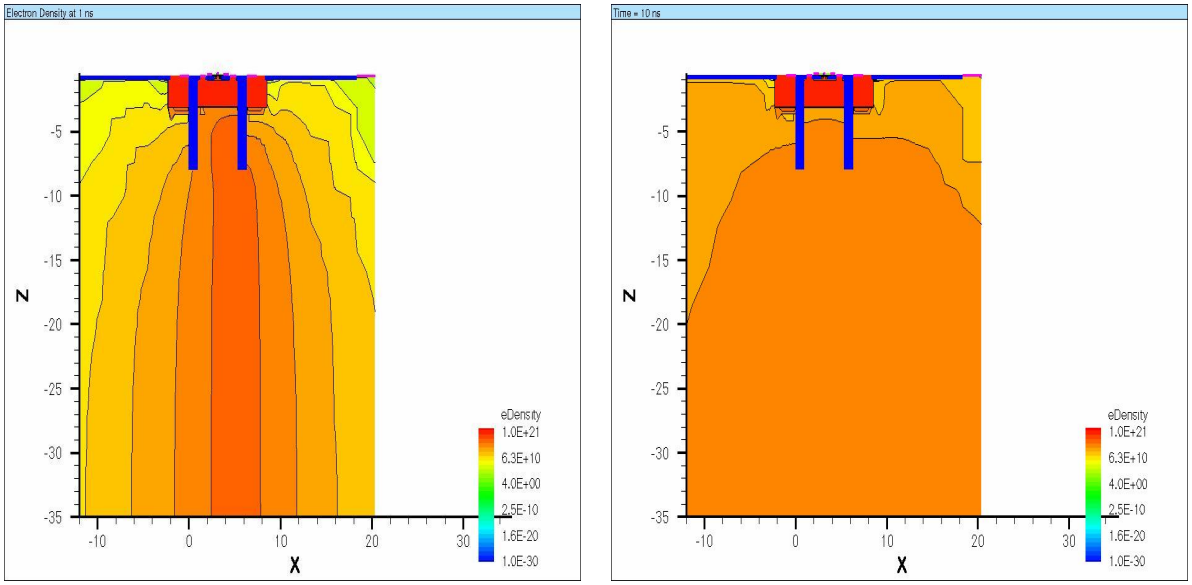


Figure 5.12: Dummy collector charge collection characteristics for ion strike at (a) emitter center (b) DT edge and (c) Outside DT between the regular and hardened HBTs.

of charge collection through diffusion. The single DT hardened HBT has a considerable reduction in charge collection than the regular and double DT hardened HBT. For the strike at x = 4.14 μm, the ion track gives rise to a heavy funnel for $\theta = 30°$ and hence we can see a heavy drift. For $\theta = 45°$, the ion track grazes the CS junction giving a less drift. For outside DT strike and for all angle of incidence, there is drift If there is a CS junction disturbance else the entire collection is through diffusion. The drift charge collection in all the locations and for all angles are completed by 2 ns.

Fig. 5.17 shows the dummy collector charge characteristics for ion strikes at angles 30° and 45°. The dummy collector junction in a single DT hardened HBT has a lateral component which is absent in double DT hardened HBT. Hence in most of the angled strike, the ion passes through the dummy CS junction. Hence we can see a drift component in most of the locations. In angled charge collection characteristics, the charge collection is mainly by diffusion in a regular HBT, and a significant reduction is achieved with hardening.



(a)Electron density contour at 1 ns (b)Electron density contour at 10 ns

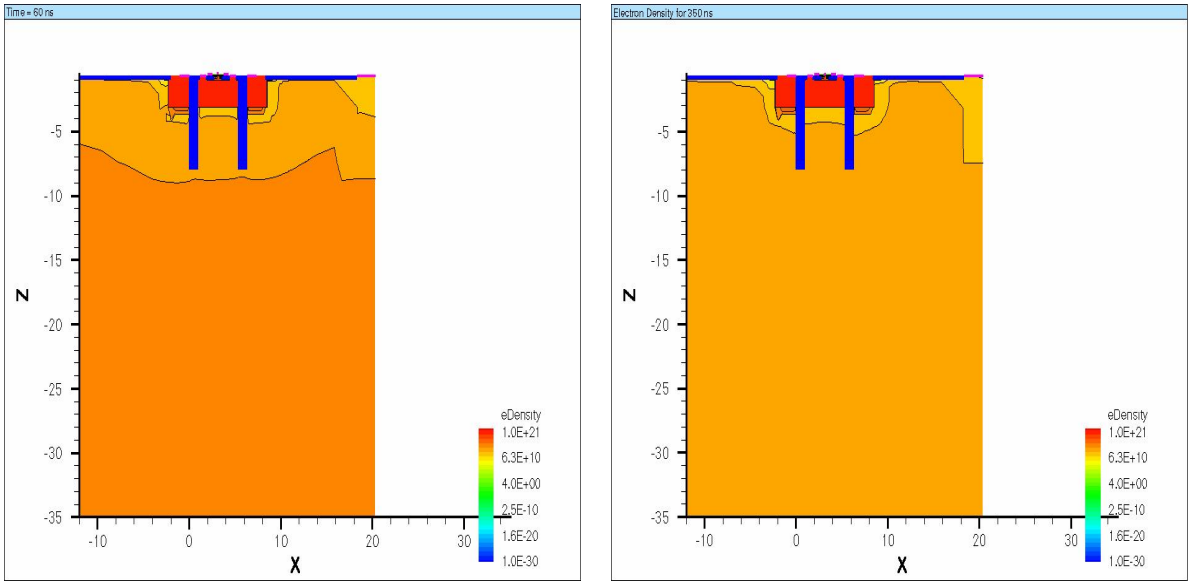
Figure 5.13: Electron density contour for an ion strike at NS Edge in a single DT hardened HBT at 1 ns and 10 ns.

Fig. 5.18 and Fig. 5.19 shows electron density contour for an ion strike at x = 4.14 μm, at an angle of incidence of 45°. The charge diffused outward from the track as time evolves. All these charges are collected by the dummy collector and reduces the charge collected by the collector.

5.7 High Resistivity Substrate

Substrate doping influences the charge collection for strikes outside DT by modifying the lifetime of the diffusing charges.

Fig. 5.20 shows charge collection comparison between substrates with doping 1×10^{15} cm^{-3} and 1×10^{14} cm^{-3}. Charge collection for $N_{sub} = 1\times10^{14}$ cm^{-3} is higher than for $N_{sub} = 1\times10^{15}$ cm^{-3} because of the slightly increased lifetime from 9 μs to 10 μs in regular and single DT hardened HBT.



(a)Electron density contour at 60 ns (b)Electron density contour at 350 ns

Figure 5.14: Electron density contour for an ion strike at NS Edge in a single DT hardened HBT at 60 ns and 350 ns.

5.8 Simultaneous Charge Collection Issues in Multiple Devices

Previous simulations are done for a stand-alone single HBT with a large simulation area of $35 \times 35 \mu m^2$. This large area is necessary due to the large lifetime and large diffusion length involved. In circuits, however, the spacing between transistors is only several microns, which is comparable to or even less than the diffusion lengths. A single ion strike can then cause simultaneous charge collection in multiple devices near the strike location [29]. Thus we need to examine charge collection using realistic layout including multiple devices. From a hardening standpoint, we do not need to pull out the individual NS layer for individual devices. Instead, the NS of several devices can be replaced by a single NS enclosing several devices, as shown below. As the ion path of angled strikes intersects with more neighbouring devices in an array of HBTs, we expect the shared dummy collector to work effectively for angled strikes and reduce charge collection in all devices. Simulation results on 2x2, 3x3 and 4x4 HBT arrays are presented below.

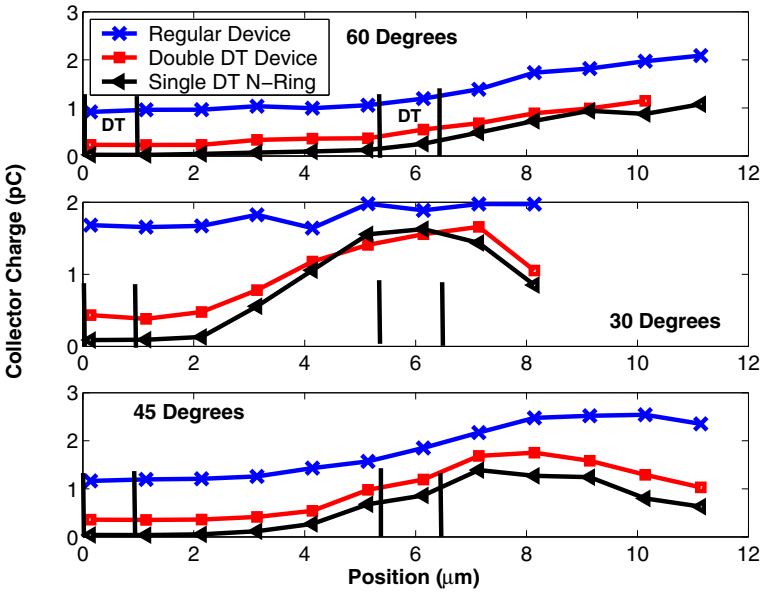
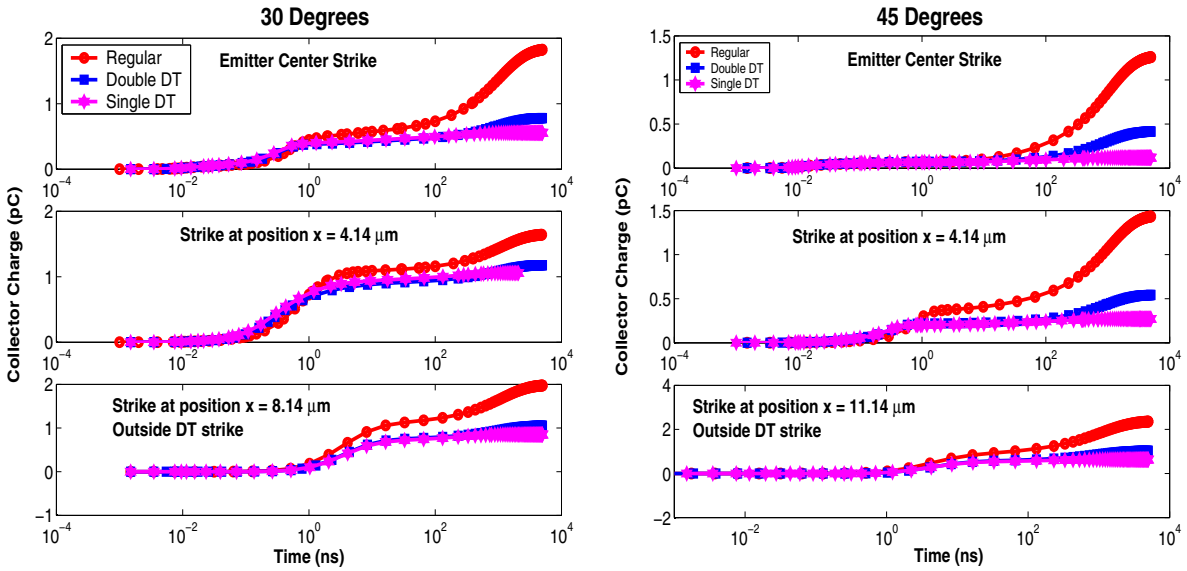


Figure 5.15: Positional charge collection comparison between the regular, single DT hardened and double DT hardened HBT for strikes at an angle of 30°, 45° and 60°.

5.8.1 2x2 HBT array

Fig. 5.21 illustrates the layout of a 2x2 array for regular and hardened HBTs simulated. C1, C2, C3 and C4 are the collectors of individual devices. A 5 μm spacing, typical of circuit layouts using SiGe HBT technology, is used. Normal ion strike simulations are performed at points A and B. Point A is at equal distance from all devices, and represents the outside DT strike location for maximum charge collection sharing. Point B is the center of C4, and represents inside DT strikes.

Fig. 5.22 gives the charge collection comparison between the regular and hardened HBT arrays for strikes at point A and B. For a strike at point A, C1, C2, C3 and C4 of the regular HBTs collect 0.7759, 0.7758, 0.735 and 0.743 pC charges, respectively. These charges are large enough to cause simultaneous upsets in all four transistors if the critical charge is less than 0.73 pC for all of the transistors in question. In the 2x2 hardened HBT array, the dummy collector collects 3.5 pC charge through drift and diffusion, thereby reducing the C1, C2, C3 and C4 charge collection to 0.0866, 0.0863, 0.0786 and 0.079 pC, respectively, and reducing event and/or error rate. Depending on propagation of transistor upset towards circuit output, the overall circuit upset



(a)Ion strike at an incidence angle of 30° (b)Ion strike at an incidence angle of 45°

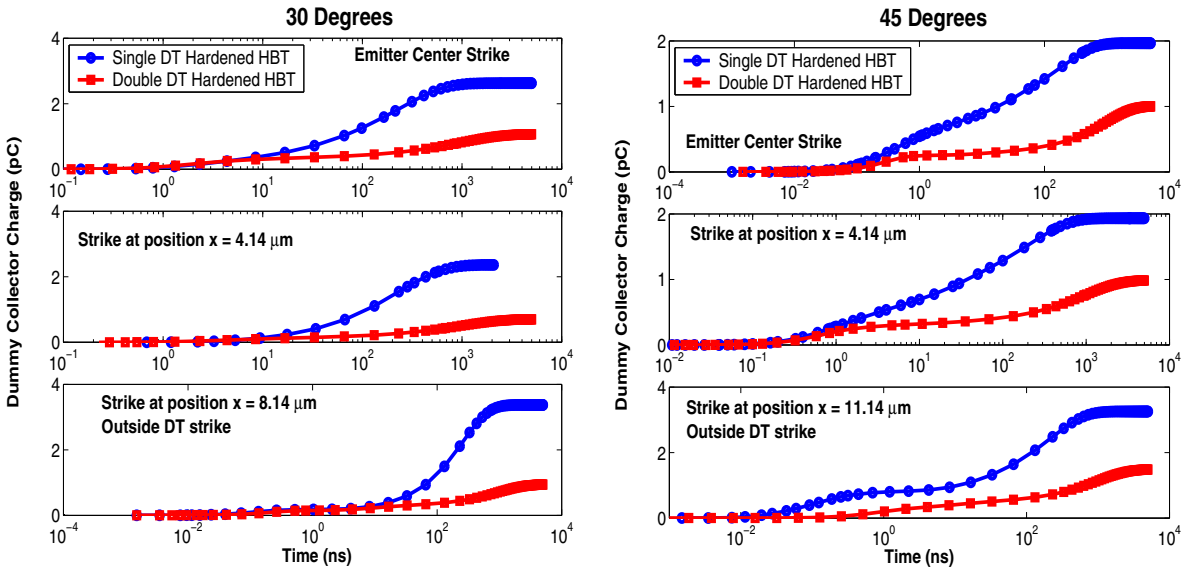
Figure 5.16: Collector charge characteristics at representative points for angle of incidence 30° and 45°.

rate should be much reduced with hardening, as all four transistors are now collecting negligible amount of charge.

For a strike at point B, the struck device C4 collects 1.7761 pC charge while C1, C2, C3 collect 0.46, 0.47 and 0.48 pC charges respectively in the regular HBT array. Even though the strike is in C4, other devices collect considerable charge through diffusion for the regular HBTs due to the long lifetimes. For a critical charge less than 0.45 pC, all of the four devices would be upset. Although the hardening approach does not significantly reduce charge collection in the struck device, it reduces the charge collection in the neighbouring devices C1, C2 and C3 down to 0.07, 0.069 and 0.058 pC, respectively, which is significant.

5.8.2 3x3 HBT array

We now examine a 3x3 array, with multiple incident angles. As illustrated in Fig. 5.23, as the angle of incidence increases, the ion path gets closer to the CS junction of adjacent devices in a regular HBT array, thereby causing more charge collection by adjacent devices. In the hardened HBT array, the ion path inevitably passes through or nearby the dummy CS junction that surrounds



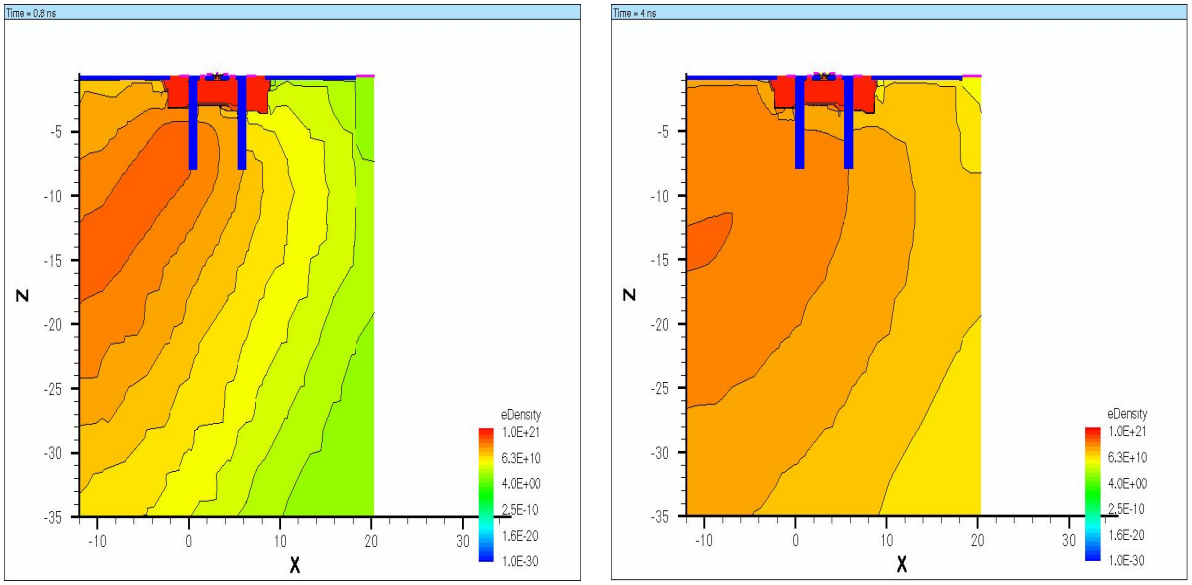
(a) Ion strike at an incidence angle of 30° (b) Ion strike at an incidence angle of 45°

Figure 5.17: Dummy collector charge characteristics at representative points for angle of incidence 30° and 45°.

all of the HBTs. This dummy CS junction shares the charge collection that was entirely collected by the collector terminal in the regular HBT array. We therefore expect a significant reduction of charge collection overall in an array of HBTs for angle strikes as well.

Fig. 5.24 and Fig. 5.25 illustrate the layout of the 3x3 regular and hardened HBT arrays. Each HBT is identified with their row and column index (i,j), i=1:3, and j=1:3. For instance, A11 refers to the HBT at row 1 and column 1. Normal, 30°, and 45° ion strike simulations are performed at three representative points 1, 2 and 3. Point 1 is at the center of A32. Point 3 is at the center of A22, also the center of the HBT array. Point 2 is located outside the DT between A32 and A22.

Fig. 5.26 shows the total charge collected by all the devices of the regular and hardened HBT array for a strike at Point 1, that is, inside the DT of A32, indicated by a red cross. A32, the struck device in the 3x3 regular HBT array collects 1.59 pC, which is less than the 1.78 pC in the 2x2 regular HBT array and 3.5 pC in the stand-alone regular HBT. This clearly shows that without hardening the charge collected by the struck device decreases with increasing HBT array size, primarily because of charge sharing by adjacent HBTs. The total charge collected by all HBTs, on the other hand, *increases* with increasing HBT array size, as expected.

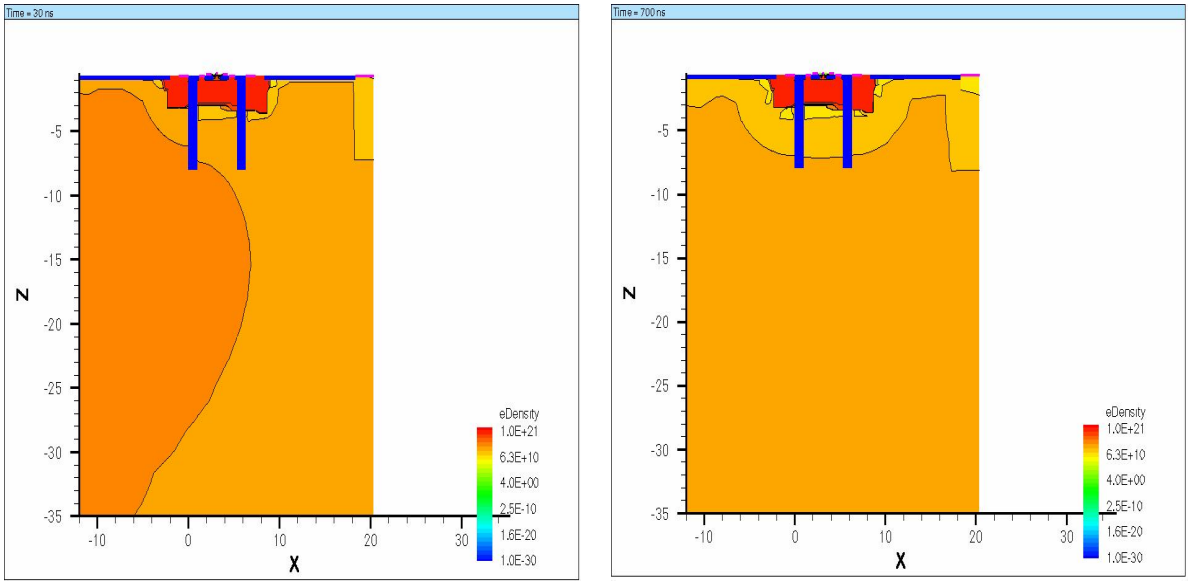


(a)Electron density contour at 0.8 ns (b)Electron density contour at 4 ns

Figure 5.18: Electron density contour for an ion strike at x = 4.14 μm in a single DT hardened HBT at 0.8 ns and 4 ns. Angle of incidence is 45°.

As in the 2x2 array, for normal and 30 degrees angle strikes, charge collection in the struck device is only slightly reduced by hardening. However, for every other device in the 3x3 array, a considerable reduction of charge collection has been achieved with hardening, as was in the 2x2 case, thanks to the presence of the dummy collector surrounding all of the HBTs. For 45 degree angle strike, a sizable reduction of charge collection in the struck device A32 is also observed and can be understood from examining how the ion path intersects different devices. Fig. 5.27 shows the total terminal charge comparison for a strike at point 3. The charge collection characteristic is similar to the charge collection at point 1.

Fig. 5.28 shows the 3x3 simulation results for a strike at Point 2, outside the DT, and in between devices A32 and A22. As charge collection is through diffusion in all of the devices in the regular HBT array, the dummy collector in the hardened HBT array yields a significant reduction in charge collection characteristic in all of the HBTs. We can therefore conclude that the shared dummy collector hardening approach works effectively for both inside and outside DT strikes, for both struck devices and neighboring devices,



(a)Electron density contour at 30 ns (b)Electron density contour at 700 ns

Figure 5.19: Electron density contour for an ion strike at x = 4.14 μm in a single DT hardened HBT at 30 ns and 700 ns. Angle of incidence is 45°.

With hardening, significant simultaneous charge collection by multiple devices is suppressed considerably, as the shared dummy collector collects a large amount of charges that would be shared by regular collectors. From the above discussions, we can see that the amount of charge collected by the struck device decreases with increasing number of adjacent devices. There is a reduction in the charge collected by the struck device due to the charge sharing between the adjacent devices.

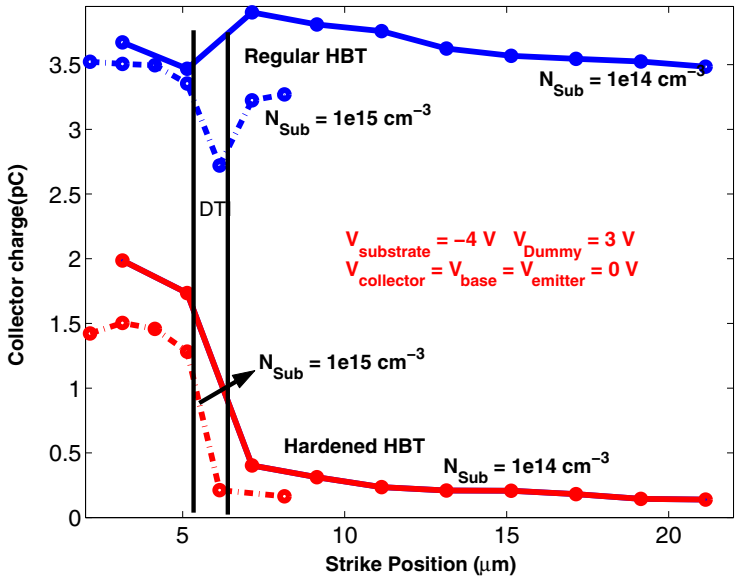


Figure 5.20: Charge collection comparison between the substrate doping of 1×10^{15} cm^{-3} and 1×10^{14} cm^{-3}. Comparison is done for regular HBT and single DT hardened HBT.

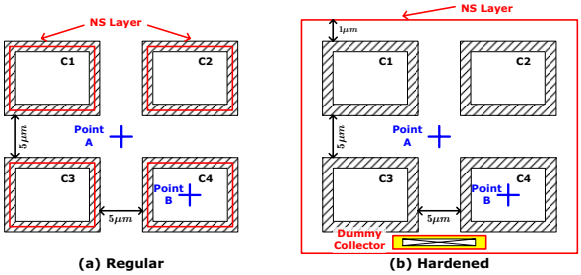


Figure 5.21: (a) 2x2 regular HBT array and (b) 2x2 hardened HBT array.

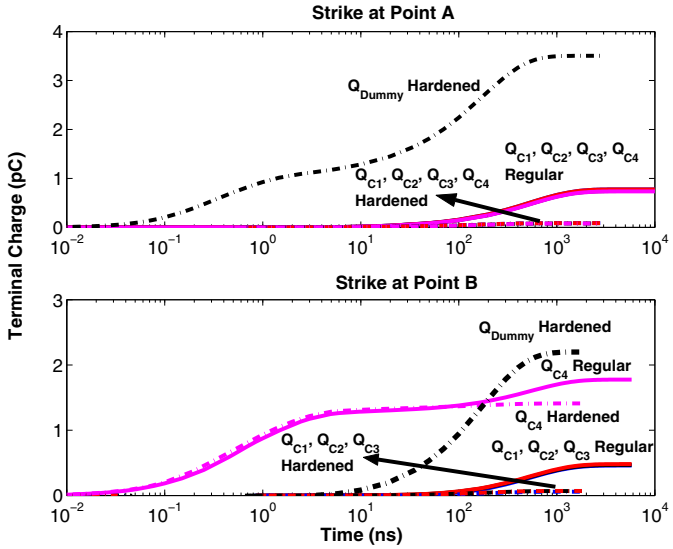


Figure 5.22: Charge collection comparison between 2x2 regular and hardened HBT arrays for ion strikes at point A and B.

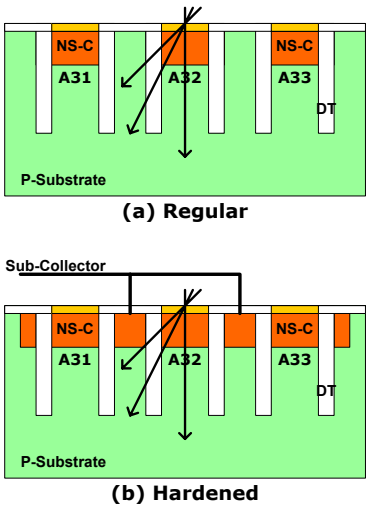


Figure 5.23: A cartoon illustration of the cross-section of the regular and hardened HBT array showing the devices A31, A32 and A33 (not to scale). The ion path represents the normal and angled strikes.

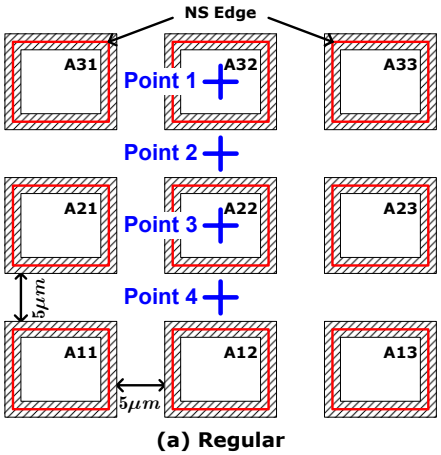


Figure 5.24: 3x3 regular HBT array.

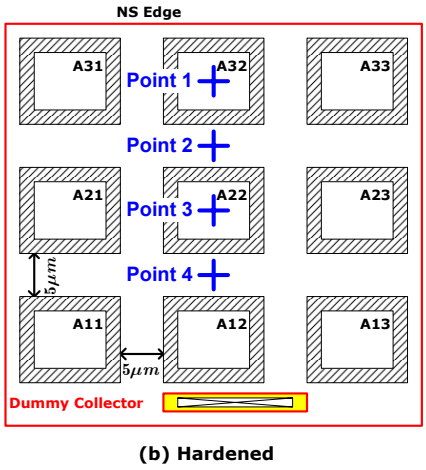


Figure 5.25: 3x3 hardened HBT array.

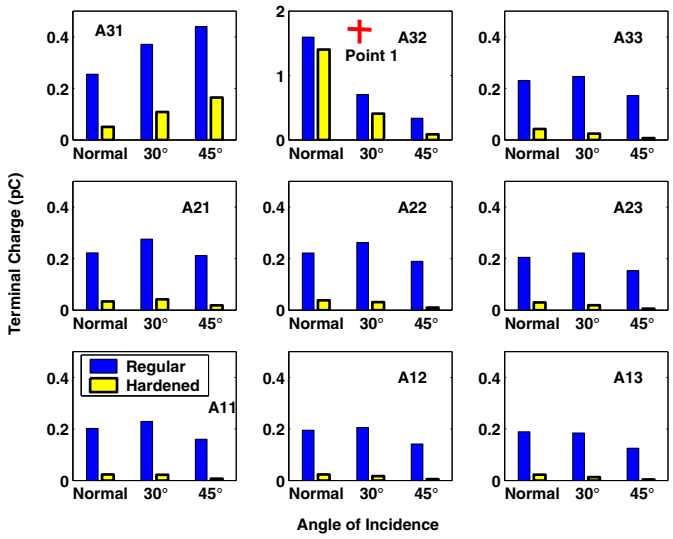


Figure 5.26: Total charge comparison between 3x3 regular and hardened HBT arrays for normal, 30° and 45° ion strikes at point 1. The red cross indicates that the device A32 is hit by the ion.

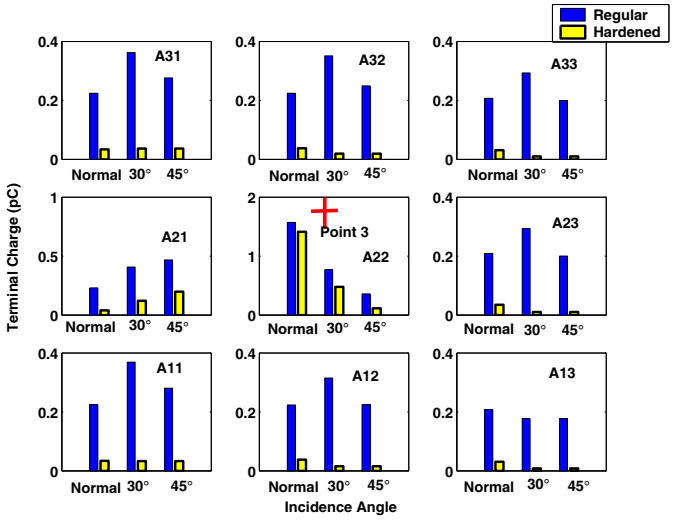


Figure 5.27: Total charge comparison between 3x3 regular and hardened HBT arrays for normal, 30° and 45° ion strikes at point 3. The red cross indicates that the device A22 is hit by the ion.

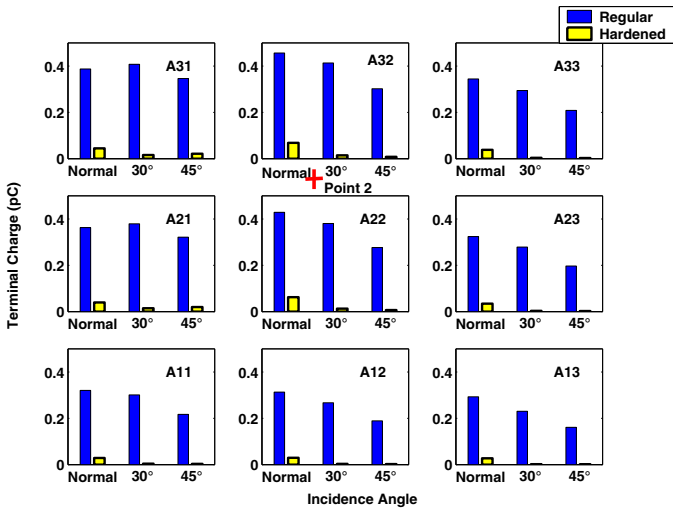


Figure 5.28: Total charge comparison between 3x3 regular and hardened HBT arrays for normal, 30° and 45° ion strikes at point 2. The red cross indicates that the ion strike position is located between A32 and A22.

Chapter 6

Mixed Mode Simulation

The simulations performed in the previous chapters were on a stand alone devices. Stand alone devices are useful only when connected in circuits. In circuits the devices have several voltage and current constraints. The device charge collection characteristic is different when connected in circuits. SEU in circuits can be studied by two methods of simulation:

- Two step simulation:

  A stand-alone device SEU transient device simulation is done. The transient current in all the terminals are saved in separate files. The circuit is designed in a circuit simulator, Cadence in our simulation. Then the current files obtained from the device simulator are fed into the particular transistor in the circuit at the specified time and the output is studied [4]. The main advantage in this type of fake simulation is that it is very fast. The disadvantage is that it is not realistic. The transient voltages and currents at different node points in the circuit will not be real.

- One step simulation:

  In the second type of simulation the circuit simulation is done in a mixed-mode device-circuit simulator, in our case DESSIS. The transistor which is struck by the heavy ion is modeled in the device level and all the other transistors are circuit models (Gummel-poon model in our case). This type of simulation takes a longer time but it is more realistic.

This chapter compares the results obtained from a fake simulation and true mixed mode simulation for a master-slave D flip flop. Also true mixed-mode simulations are performed on analog emitter follower circuits. In the analog emitter follower circuit the collector is at the supply potential and

the emitter is at lower potential. There is a shunt of the collector and the emitter terminal. The collector to emitter shunt current is complex due to the device/circuit interactions. Mixed mode simulations better capture the device/circuit interactions. The mixed mode simulations neglects charge sharing when multiple devices are present.

6.1 Simulation Details

In DESSIS all the circuit elements are described by a Gummel-Poon model i.e. DESSIS accepts only Gummel-Poon model for active and passive elements in circuit. The Gummel-Poon model is obtained in 2 steps. First the VBIC model of the device is obtained from Cadence. Then the Gummel-Poon model is obtained from the conversion formula between the VBIC and Gummel-Poon models. The device that was struck is modeled as a separate three dimensional device and all other devices, passive elements are specified by the compact models. The presence of both device level and circuit level models in the same circuit is called as the mixed mode simulation. The simulation was performed for a Master-Slave D flip flop and analog emitter follower. The D-FlipFlop two step SEU simulation was performed in Cadence. In Cadence the simulation was performed as follows. The transient currents for an emitter center strike in single device simulation is saved and are fed into the device that is struck by the ion. A transient simulation is performed in cadence. The results are compared with the DESSIS mixed mode simulation.

6.2 Current Mode Logic D-FlipFlop Simulation

A rising edge-triggered master-slave D flip flop was used to study the SEU in circuits. The transistors used in the D flip flop is the IBM 5HP SiGe HBT. The D flip flop is a basic building block of the 32-stage shift register. Fig. 6.1 is the master-slave flipflop used in the simulation. The master stage consists of a pass cell (Q_1 and Q_2), a storage cell (Q_3 and Q_4), a clocking stage (Q_5 and Q_6) and a control switch (Q_7). The slave stage has a similar circuit configuration. The transistors in the pass and storage cells are stacked over the CLK and control transistors. Hence, the input levels at the clock stage and the control have to be level shifted for the transistors to operate

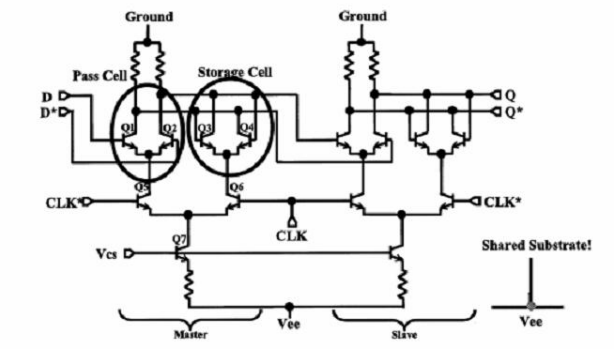


Figure 6.1: Master-Slave D-Flipflop used in mixed mode simulation.

in the forward active mode while conducting. The storage cell of the master stage and and the pass cell of the slave stage are controlled by CLK and the pass cell of the master stage and the storage cell of the slave stage are controlled by CLK*. The transistor in the storage cell of the master was struck. The transistors in the storage cell is a very sensitive transistor in the circuit. In DESSIS, the struck transistor is modeled in the device level and all other passive and active components of the circuit are modeled using the Gummel-Poon model. Gummel Plots from Cadence is compared with the DESSIS Gummel Poon model. An LET of 0.037 pC/μm was used which is equivalent to 3.7 $MeV - cm^2/mg$. The strike is a deep strike, where the ion passes through the entire device. The SEU currents have to be activated within the circuit hold time right after the clock goes from low to high. This is a sensitive time instant for induced transient currents to produce an upset at the output. The SEU currents are activated at 1.5 ns in our simulation.

Fig. 6.2 gives output waveform for the cadence simulation. We can clearly see an SEU for one period. We can clearly observe a cross coupling between the transistors Q_3 and Q_4 at the transistor level in Fig. 6.1. The base and collector of Q_3 is connected to collector and base of Q_4, respectively. A positive feedback is produced between Q_3 and Q_4 due to the cross coupling, which is required for proper circuit function. However, the upset produced in one output due to the ion strike in one of the transistors causes an upset in the complementary output due to the cross coupling between the transistors. Fig. 6.3 gives output waveform from the device simulator DESSIS. The output waveforms, Q and Qbar, from Cadence and DESSIS simulator are approximately equivalent. In

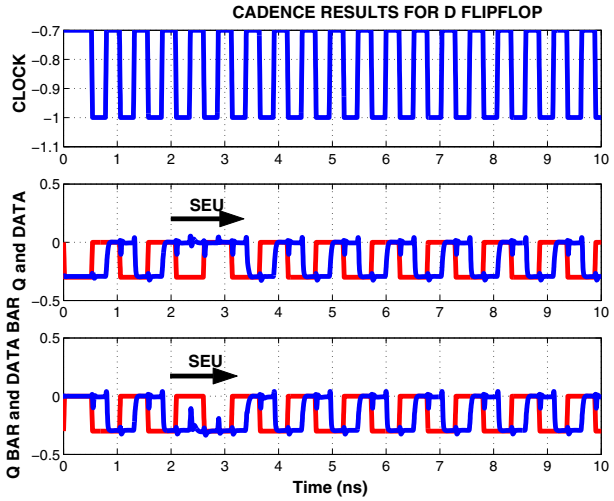


Figure 6.2: Output waveforms of the D flip flop for the Cadence simulation.

both Cadence and DESSIS, SEU lasts for one period in the output. The magnitude of the output voltage levels are the same in DESSIS and Cadence. The SET voltage change in the output waveform is due to the CS junction drift and CB junction drift charge collection. The voltage change introduced by the CS junction diffusion charge collection is negligible. Such voltage change is restored by the circuit operation and no SEU is produced. The CB drift charge is shown to be more effective than the CS drift charge collection [33].

6.3 Analog Emitter Follower

Analog emitter follower is simulated using DESSIS mixed mode simulation. In the emitter follower the most important is the output voltage which relates to the emitter current. Hence this circuit relies on the emitter current not the collector current. So we will need a 1 step true mixed mode as there is likely a short circuit current between emitter and collector. We do not know how much which we need to examine through the simulations. The transistor used in this simulation is the 0.18×3.00 8HP SiGe HBT. Three different analog emitter followers are simulated. The impedance seen by the emitter is varied in the three circuits and also the bias current is varied for the three circuits. The charge collection depends on the impedance seen by the emitter and

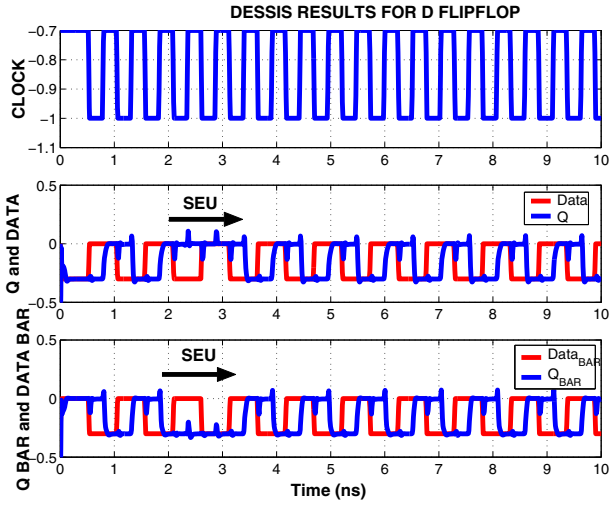


Figure 6.3: Output waveforms of the D flipflop for the DESSIS simulation.

collector terminals in a circuit. Hence three different circuits are simulated. For these simulations an LET of 0.1 pC/μm was used and the strike is a deep strike passing through the entire device. The default parameters for bulk SRH was used and the surface SRH was switched off. The ion strike position is at the center of the emitter because the ion should pass through the CB junction. The charge generated by the ion strike gets collected by the base through drift through the CB junction field. The emitter voltage disturbance simply follows the disturbance in the base voltage by the charge collection in the base terminal.

6.3.1 Circuit 1

Fig. 6.4 is shows a schematic of an analog emitter follower. The substrate is grounded. The bias current in this circuit is 1.1 mA. The collector is connected to a supply voltage of 3.3 V. The emitter is connected to two 4 K resistors parallel to each other. The steady state values for emitter, collector, substrate and base currents are -1.134 mA, 1.132 mA, -5.376 fA and 2.089 μA respectively. The EF current given in the figure is the emitter current during steady state operation. An emitter current of 1.134 mA and two parallel 4 K resistors in the emitter terminal gives a steady emitter voltage of 2.2 V.

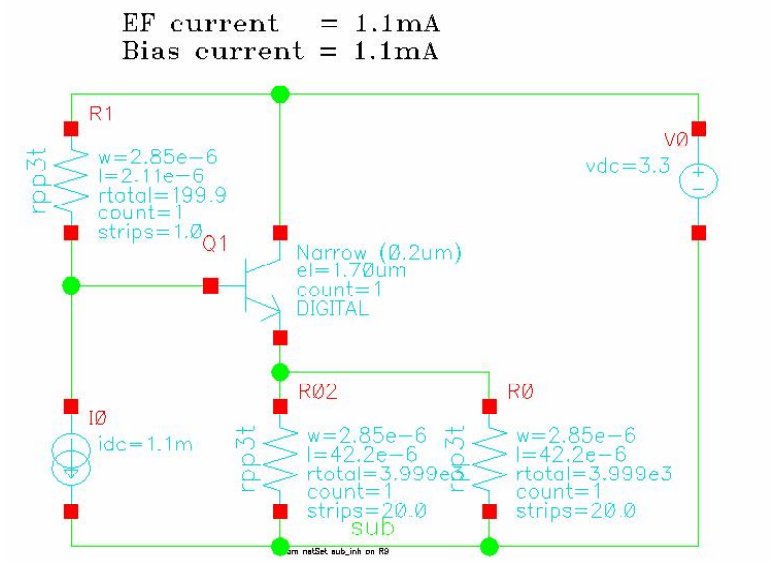


Figure 6.4: Analog Emitter Follower(circuit 1). Substrate is grounded.

Fig. 6.5a shows the terminal currents in circuit 1 after the ion strike, in log scale. This terminal current is the sum of the steady state current and the SEU current.

$$I_{Total} = I_{Steady} + I_{SEU}$$

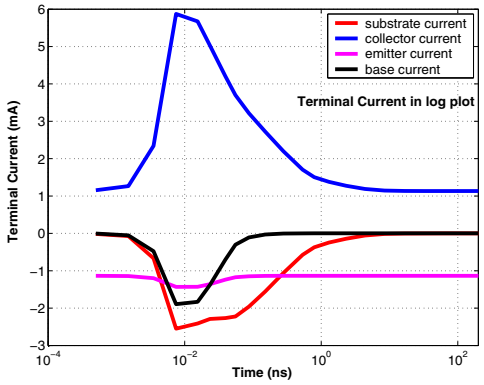
and Fig. 6.5b shows the SEU terminal current which is

$$I_{SEU} = I_{Total} - I_{Steady}$$

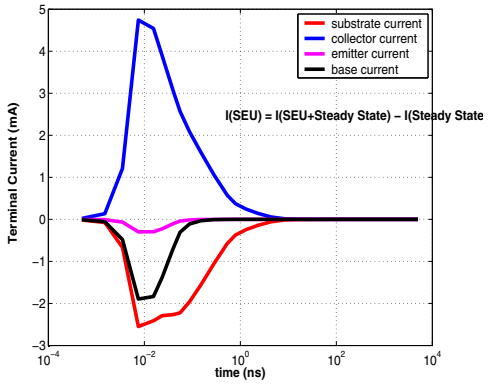
.

Fig. 6.5b clearly shows that the emitter and base transient currents decay at 0.09 ns, which is purely due to the drift current from the CB junction. The collector current and the substrate current contains both the drift and diffusion components from the CS junction. Fig. 6.6a and b gives the total terminal current and the SEU terminal current respectively in linear scale.

Fig. 6.7 gives the emitter terminal current in log scale and linear scale. Inn the emitter follower, the collector terminal is at the supply potential, which is 3.3 V in our case. As seen in Fig. 6.8, the emitter terminal reaches a maximum voltage of 2.88 V during the ion strike. Hence we can see that the emitter terminal is at a lower potential than the collector terminal always.

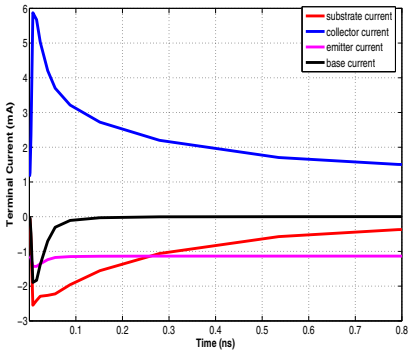


(a) Terminal currents of circuit 1 in log scale

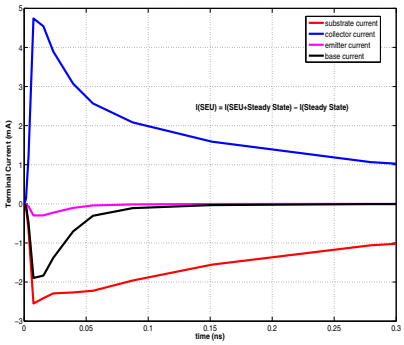


(b) Terminal SEU currents of circuit 1 in log scale

Figure 6.5: Terminal currents of circuit 1, which is the sum of the steady state current and SEU current and terminal SEU current of circuit 1 in log scale.



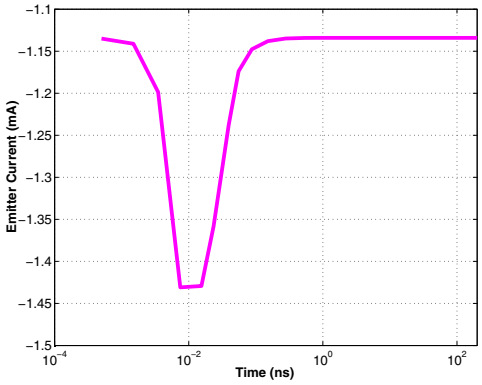
(a) Terminal currents of circuit 1 in linear scale



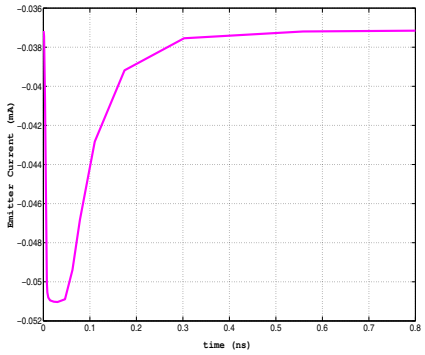
(b) Terminal SEU currents of circuit 1 in linear scale

Figure 6.6: Terminal currents of circuit 1, which is the sum of the steady state current and SEU current and terminal SEU current of circuit 1 in linear scale.

Hence there is a shunt of collector and emitter. The shunt current goes from the higher potential (collector) to the lower potential (emitter). So we see a negative current in the emitter terminal. As soon as the electrons leave, the shunt breaks up and acts like an open circuit. The impedance also plays a role in charge collection. Collector sees zero impedance to ground, while Emitter sees some impedance. The emitter votage time scale of SEU is 0.2ns, which is much shorter compared to the funneling time which is approximately 0.3ns. Hence the emitter voltage SET is mainly due to the drift collection from CB/CS junctions.

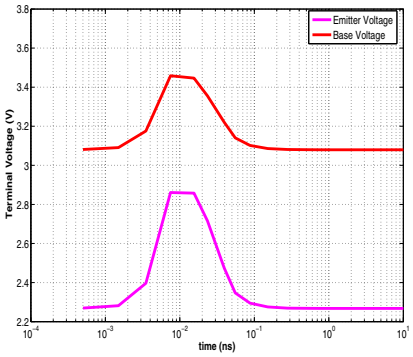


(a) Emitter terminal current for circuit 1 in log scale

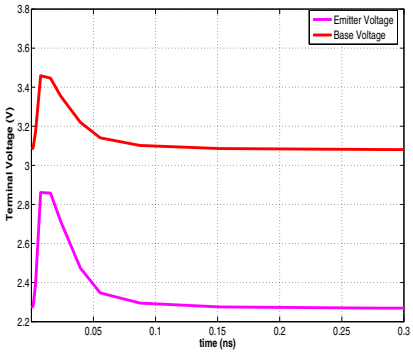


(b) Emitter terminal current for circuit 1 in linear scale

Figure 6.7: Emitter terminal current of circuit 1.



(a) Base and emitter voltage for circuit 1 in log scale



(b) Base and emitter voltage for circuit 1 in linear scale

Figure 6.8: Base and emitter voltage of circuit 1.

6.3.2 Circuit 2

Fig. 6.9 gives the second circuit of an analog emitter follower. The bias current for the circuit is 140 μA. The collector is connected to a supply voltage of 3.3 V. The emitter terminal is connected to a 64 K resistor. The steady state values for emitter, collector, substrate and base currents are -37.14 μA, 37.11 μA, -5.380 fA and 27.43 nA respectively. An emitter current of 37.14 μA and a resistor of 64 K connected to the emitter terminal gives rise to an emitter steady state voltage of 2.377 V. The impedance seen by the emitter in the previous circuit is 2 K while in the second circuit it is 64 K. There is a 32 times increase in the impedance seen by the emitter in the second circuit. But the emitter current in the second circuit is 32 times less than the first circuit. Hence the steady state emitter voltage is approximately the same in both the circuits.

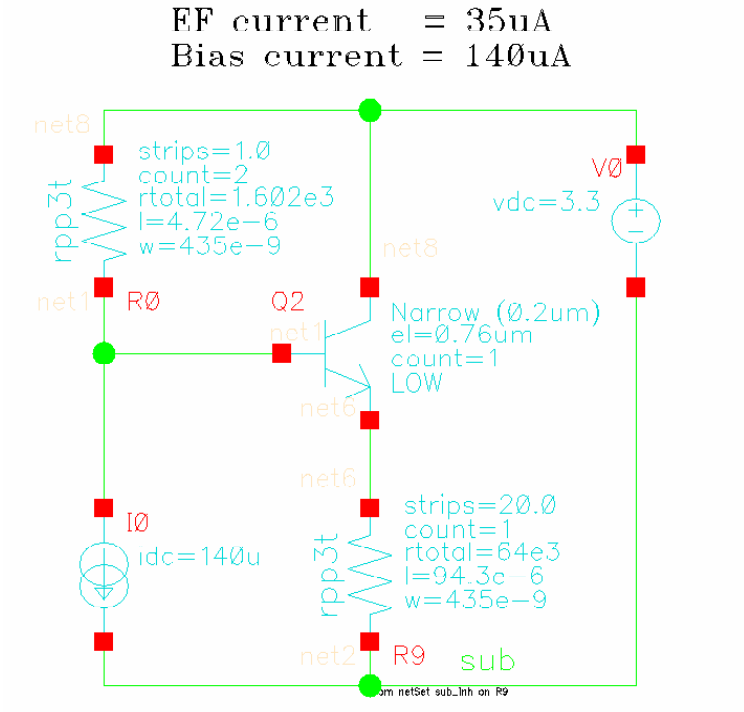
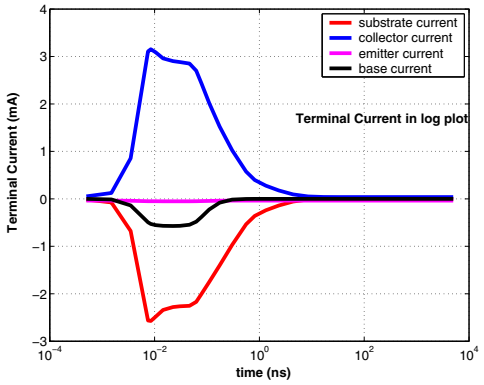
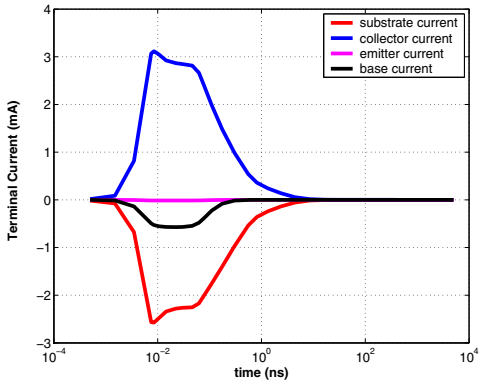


Figure 6.9: Analog Emitter Follower(circuit 2).

Fig. 6.10a and b gives the total terminal current and the SEU current respectively. The total terminal current is the sum of the steady state current and the SEU current. Fig. 6.11 gives the total terminal current and SEU current in linear scale. In the previous circuit (circuit 1) the impedance seen by the emitter is two parallel 4 K resistors but in circuit 2 the impedance seen by the emitter terminal is a 64 K resistor. Fig. 6.12 gives the emitter current in log and linear scale. The collector terminal is at 3.3 V and from Fig. 6.13 we can see that the maximum voltage reached by the emitter terminal is 3.266 V, which is less than the collector voltage. Hence the explanation given in the previous section holds good for this circuit also. There is a shunt of the collector and the emitter terminal, which leads to a current flow from the collector to the emitter terminal. The voltage rise in the second circuit due to SEU is to 3.266 V but the voltage rise in circuit 1 due to SEU is to 2.86 V.

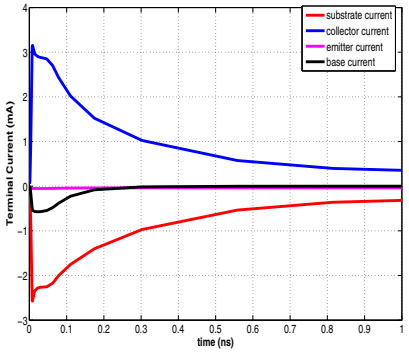


(a) Terminal currents of circuit 2 in log scale

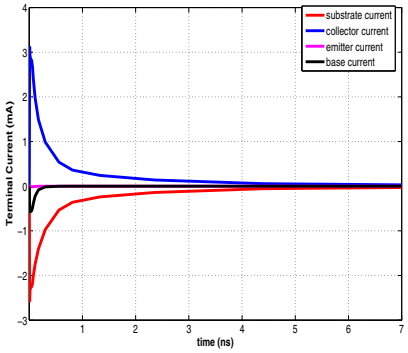


(b) Terminal SEU currents of circuit 2 in log scale

Figure 6.10: Terminal currents of circuit 2, which is the sum of the steady state current and SEU current and terminal SEU current of circuit 2 in log scale.



(a) Terminal currents of circuit 2 in linear scale



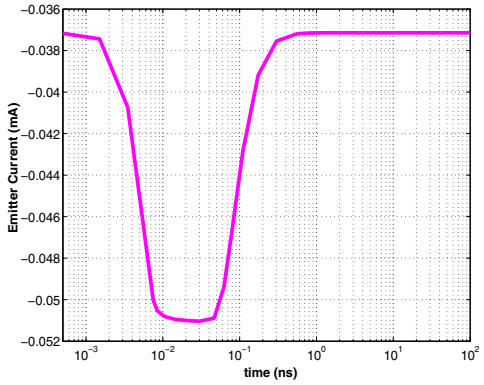
(b) Terminal SEU currents of circuit 2 in linear scale

Figure 6.11: Terminal currents of circuit 2, which is the sum of the steady state current and SEU current and terminal SEU current of circuit 2 in linear scale.

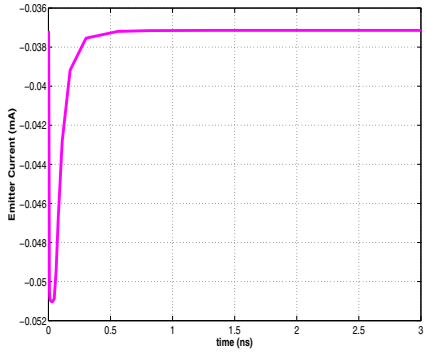
6.3.3 Circuit 3

Fig. 6.14 shows circuit 3 of the analog emitter follower. The steady state values for emitter, collector, substrate and base currents are -37.14 μA, 37.11 μA, -5.379 fA and 27.43 nA respectively. The steady state emitter voltage is same as the previous two circuits, which is approximately 2.7 V.

Fig. 6.15a and b shows the total terminal current and SEU current respectively for circuit 3. Fig. 6.16 shows the total terminal current and SEU current in linear scale. Fig. 6.17 gives the emitter current in log scale and linear scale for circuit 3. As in the previous 2 circuits, the emitter terminal reaches a maximum of 3.284 V which can be seen from Fig. 6.18. This is less than the

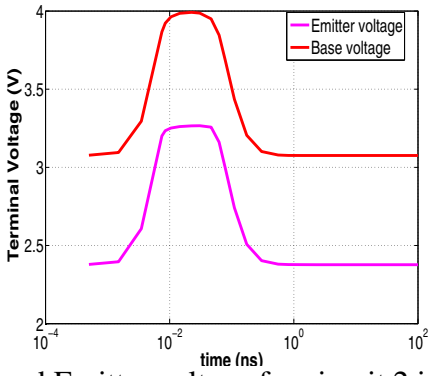


(a) Emitter terminal current for circuit 2 in log scale

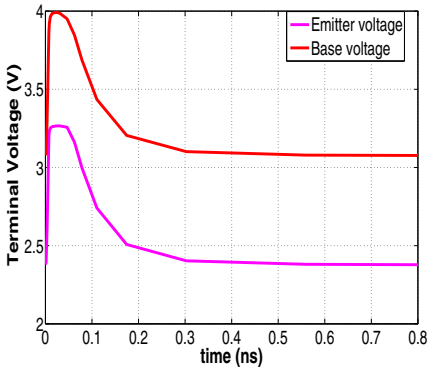


(b) Emitter terminal current for circuit 2 in linear scale

Figure 6.12: Emitter terminal current of circuit 2.



(a) Base and Emitter voltage for circuit 2 in log scale



(b) Base and Emitter voltage for circuit 2 in linear scale

Figure 6.13: Base and emitter voltage of circuit 2.

collector terminal which is at 3.3 V. Hence the explanation given for the previous two circuits hold good for this circuit also.

6.4 Comparison between three circuits

Table 6.1: Design Parameters for three typical emitter followers.

Circuit	I_{EF}	RBB	I_{DC}	REE
Circuit1	1.1 mA	200	1.1 mA	2000
Circuit2	35 μA	64000	140 μA	1600
Circuit3	35 μA	64000	70 μA	3200

The table above gives the design parameters for the three analog emitter followers. Fig. 6.19 and Fig. 6.20 shows the base voltage and emitter voltage comparison between the three circuits.

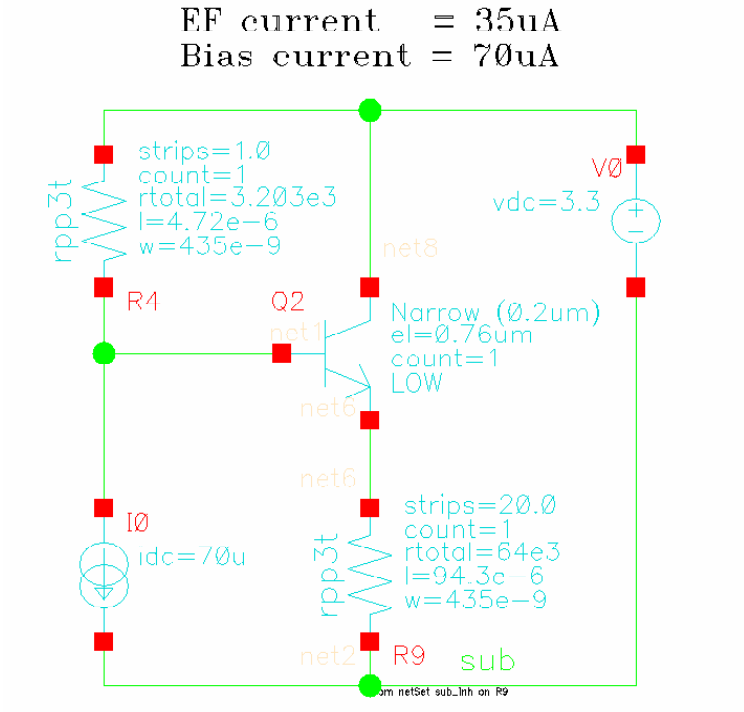


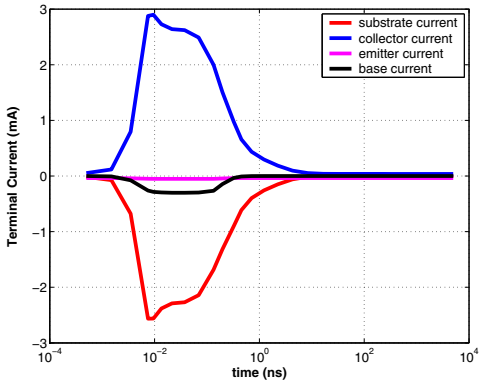
Figure 6.14: Analog Emitter Follower(circuit 3).

In circuit 1, the emitter resistance is 2000 ohms effectively and the base resistance is 200 ohms. In circuit 2 and circuit 3, the base resistance is 64 Kohms but the emitter resistance in circuit 2 is 1600 ohms and 3200 ohms in circuit 3. From the voltage comparison figures, the transient base voltage is almost same for circuit 2 and circuit 3 irrespective of 2X difference in the emitter resistance and IEF constant. Hence we can say that the emitter resistance doesn't play too big a role in SET voltages. The emitter voltage follows the base voltage due to the circuit operation constraints [34].

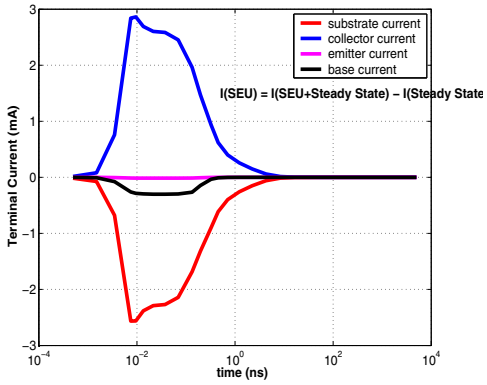
Fig. 6.21 and Fig. 6.22 shows the base current and emitter current comparison between the three circuits. The base current is also not too different in circuit 2 and circuit 3. The emitter current follows the base current due to circuit constraints.

6.5 Conclusion

The Current Mode Logic Master-Slave D-flipflop was simulated using both mixed mode simulation in DESSIS and in Cadence. Both produced the single event upset for the same time period.

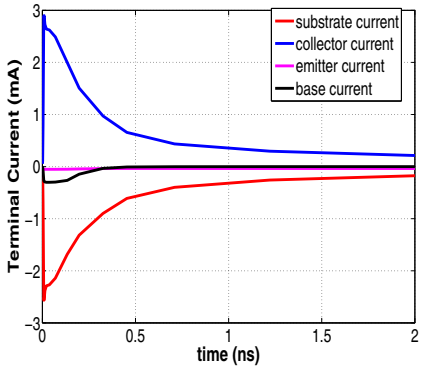


(a) Terminal currents of circuit 3 in log scale

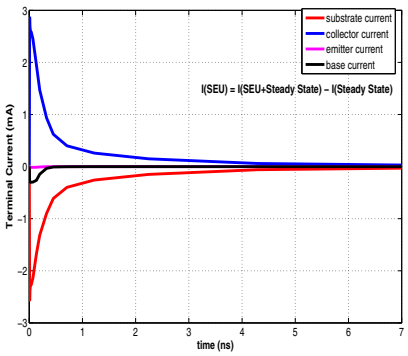


(b) Terminal SEU currents of circuit 3 in log scale

Figure 6.15: Terminal currents of circuit 3, which is the sum of the steady state current and SEU current and terminal SEU current of circuit 3 in log scale.



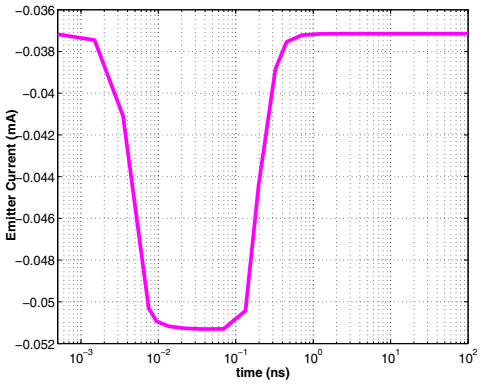
(a) Terminal currents of circuit 3 in linear scale



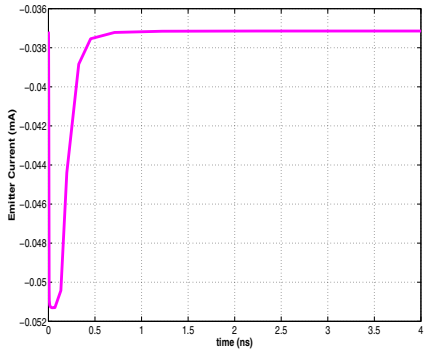
(b) Terminal SEU currents of circuit 3 in linear scale

Figure 6.16: Terminal currents of circuit 3, which is the sum of the steady state current and SEU current and terminal SEU current of circuit 3 in linear scale.

The collector-base and collector substrate drift charge collection are the primary cause for SEU. Three analog emitter follower circuits were simulated using mixed mode simulation with three different design parameters. The base voltage/base current is primary cause for SEU because of the charge collection from CB junction. The emitter terminal simply follows the disturbance in the base terminal due to the circuit operation and constraints. The base resistance RBB also plays a major role in SEU. The product of SEE induced base current and RBB determines the base voltage upset and the emitter voltage upset tracks the base voltage upset.

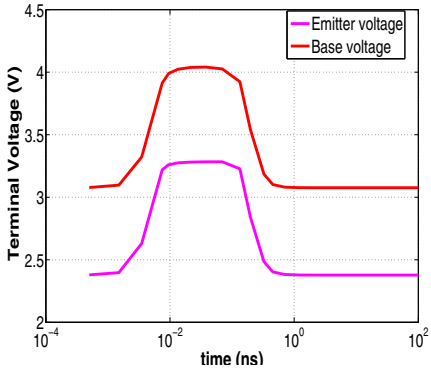


(a) Emitter terminal current for circuit 3 in log scale

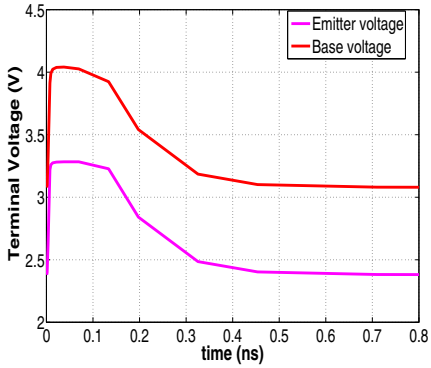


(b) Emitter terminal current for circuit 3 in linear scale

Figure 6.17: Emitter terminal current of circuit 3.



(a) Base and emitter voltage for circuit 3 in log scale



(b) Base and emitter voltage for circuit 3 in linear scale

Figure 6.18: Base and emitter voltage of circuit 3.

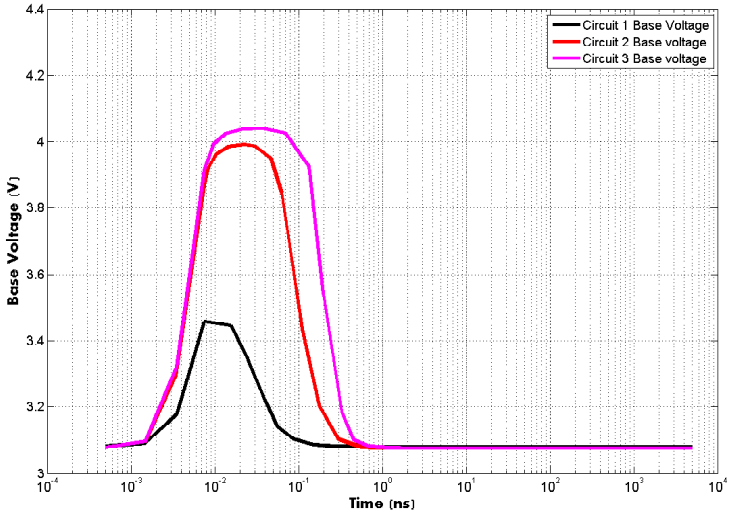


Figure 6.19: Transient Base voltage comparison between the three analog emitter follower circuits.

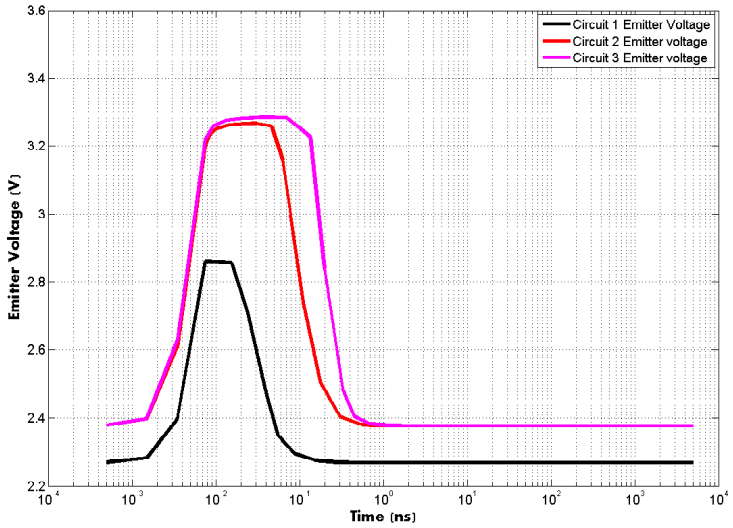


Figure 6.20: Transient Emitter voltage comparison between the three analog emitter follower circuits.

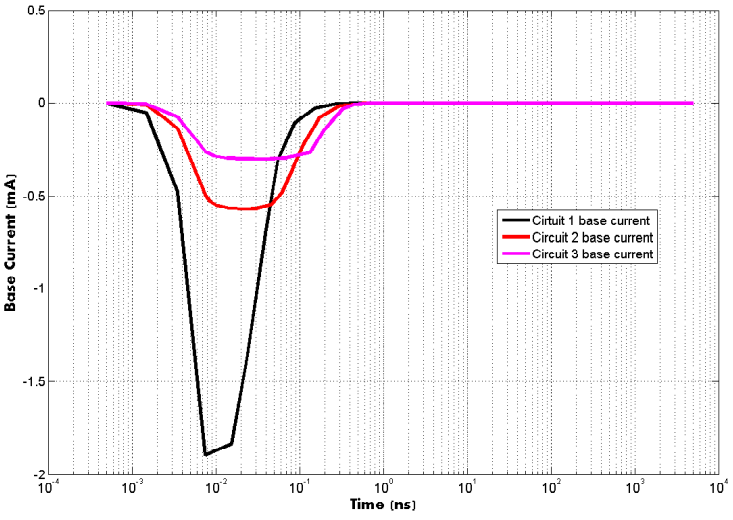


Figure 6.21: Transient Base current comparison between the three analog emitter follower circuits.

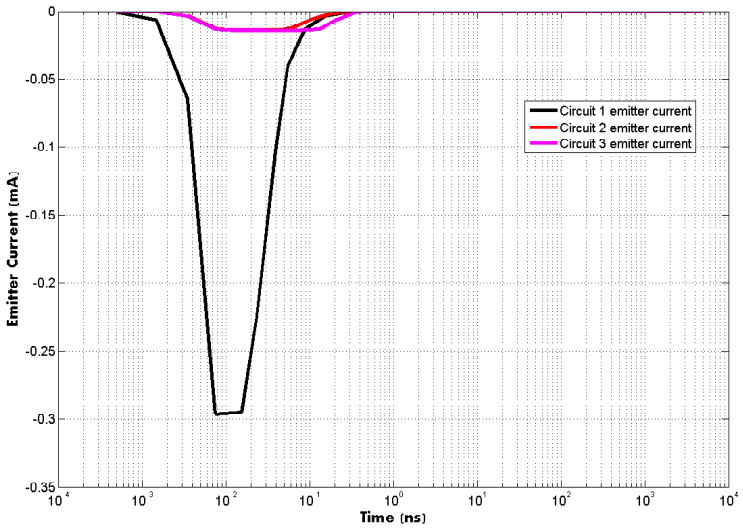


Figure 6.22: Transient Emitter current comparison between the three analog emitter follower circuits.

Chapter 7

Conclusion and Future Work

Single event upset was simulated in 5HP and 8HP SiGe HBTs. The ion strike simulation position on the device was varied and the positional dependence of charge collection was studied. The simulated data was compared with the microbeam data from sandia labs. The 5HP HBT simulated data was a good fit with the microbeam data. Although the 8HP was not a good fit, the simulated data followed the trend in the microbeam data. The charge collection was maximum for a strike at the emitter center and rolled off for strikes outside DT.

The CS junction which plays a major role in charge collection was replaced with a buried oxide, which is SiGe HBT on SOI. This type of hardening is called as Radiation Hardening By Process (RHBP), where there are changes in the process. The intrinsic part of the device is the same as in the bulk. It was found that the charge collection was independent of the Si film thickness above the buried oxide. The charge collection in the SOI HBT is much reduced than the bulk HBT. This reduction in charge collection is due to the reduced charge collection by the collector and substrate terminal in the SOI HBT. The base and emitter terminal charge collection is approximately equal in bulk and SOI HBT.

Another type of hardening is Radiation Hardening By Design (RHBD), where the changes are made in the layout. An extra dummy collector is introduced outside the deep trench, surrounding the deep trench isolation. This dummy collector reduces the diffusive charge collected by the collector terminal in the regular HBT. In a circuit, this dummy collector can be filled in the space between devices in the layout. Charge collection is studied in 2×2 and 3×3 HBT arrays. The charge collection has been compared between the regular and dummy collector HBT array. The dummy CS junction reduces the diffusive charge collection by considerable amount thereby preventing simultaneous charge collection in multiple HBT arrays. The amount of charge collected by

the struck device in a HBT array decreases with increasing number adjacent devices due to sharing of charge collection.

Single event upset when the devices are in a circuit are studied. Mixed mode simulation is performed on a Master/Slave D-Flip Flop. Fake mixed mode and true mixed mode simulations are compared for the D-flip flop. The output waveforms are similar for the true mixed mode and the fake mixed mode simulation. True mixed mode simulations are done for analog emitter follower and the waveforms are studied.

7.1 Future Work

Mixed mode simulations were not extensive in this work. The difference between the true mixed mode and fake mixed mode simulations can be performed for other type of circuits and waveforms can be compared. The dummy collector device and the SOI device can be introduced in circuits and the output can be compared with the circuits with regular devices. The simulation data can be compared with measured data for the radiation hardened device.

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